Journal of Magnetics 7(3), 101-105 (2002)

MTJ based MRAM Core Cell

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(Received 19 August 2002)

MRAM (Magnetoresistive Random Access Memory) is a promising candidate for a universal memory that meets all application needs with non-volatile, fast operational speed, and low power consumption. The simplest architecture of MRAM cell is a series of MTJ (Magnetic Tunnel Junction) as a data storage part and MOS transistor as a data selection part. This paper is for testing the actual electrical parameters to adopt MRAM technology in the semiconductor based memory device. The discussed topics are an actual integration of MRAM core cell and its properties such as electrical tuning of MOS/MTJ for data sensing and control of magnetic switching for data writing. It will be also tested that limits of the MRAM technology for a high density memory.

Key words : MRAM (Magneto-resistive Random Access Memory), GMR (Giant Magneto-resistance), MTJ (Magnetic Tunnel Junction)

1. Introduction

Semiconductor memory devices those are currently used in most electronic applications have very distinct attributes, therefore, each memory could be used only for limited applications. For example, DRAM is a high-speed and high-density memory, but has disadvantages of high power and volatility. FLASH memory is a non-volatile memory with low power, but has disadvantages of bad endurability and low speed. SRAM is a high speed and low power memory, but has relatively low density. To implement all the advantages into a universal memory, many researchers have worked on new memories such as FeRAM, MRAM, OUM, and STTM. These new memory devices could substitute conventional memories or they could bring a new market. Among those new memories, MRAM (Magnetic Random Access Memory) using GMR (Giant Magnetoresistance) technology is a promising candidate for a universal memory with non-volatility, high speed, high density, and low power.

The introduction of giant magneto-resistance (GMR) that was discovered in magnetic/non-magnetic multilayer in 1988 [1], has been a major impetus to attribute magneto-resistive random access memory (MRAM), new technology of memory device. Once having the GMR technologies, two magnetization states, magnetization parallel and anti-parallel, are controllable and the resistance difference between two states reaches within a comparable range of commonly using semiconductor memory technology. The major impact of MRAM is its long storage lifetime by non-volatility, low cost and lack of any wear-out mechanism.

Honeywell Corporation has successfully demonstrated MRAM with the memory elements of core cell of a current-in-plane (CIP) spin valve structure that is not effective for high MR value, density capability, and operating speed [2].

To overcome those discrepancies, a different approach has been introduced to MRAM by exploiting another manifestation of spin-polarized transport. This approach is using spin dependent tunneling technology through an oxide barrier between two ferromagnetic thin films where the magnetization controls by exchange biasing due to introduce an anti-ferromagnetic layer. The magnetic tunnel junction (MTJ) quickly generates the memory elements of core cell with MOS transistor as a switch to select a data location.

The advantages of MTJ for MRAM core cell are high magneto-resistance (MR) and resistance compatibility

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with the semiconductor devices. With current-perpendicular-to-the plane (CPP) structure of MTJ, every electron passes through all the magnetic layers whose magnetization states are well controlled by the exchange-bias spin valve (EBSV). Employing of an oxide barrier allows MTJ to make series connection with MOS transistor without MR loss by the channel resistance of MOS transistor. Fortunately, very thin layer of AlO_x as a barrier material and its interfaces with ferromagnetic layers don't have lots of scattering centers of spin flip.

Application of MTJ allows a simple core cell architecture that is very close to those of semiconductor memory. This architecture scheme opens a potential technology of universal memory by MRAM for both of stand alone and embedded memory application. IBM and Motorola have recently demonstrated MRAM technology with compatible performances and some reasonable density [3, 4].

Successful demonstration by the previous work ensures that MRAM technology is a strong candidate of universal memory among the other new memory technologies with the comparison topics such as power consumption, speed, scalability, retention, endurance, and density. However there are still some fundamental issues to attain a real memory device.

In this paper, we simplify the cell structure to test fundamental limitation of MRAM technology as well as core cell performance. Now the selected issues will be listed and discussed in detail.

2. Core Cell Integration

MRAM core cell attributes to a hybrid technology of the CMOS and the MTJ process where the MTJ is connected to the MOS transistor in series. Figure 1 shows an example of the MTJ that is composed of two crossing lines – a write line and a bit line, and a patterned multilayer stack composed of a Ru buffer, IrMn as an antiferromagnetic layer, CoFe as a pinned layer, plasma oxidized AlO_x as a tunnel barrier, Py(NiFe) as a free layer, and a capping layer.

The tested MTJs show 23~34% of MR, and 1 k~2 $M\Omega\mu m^2$ of AR (Area times Resistance). Since AR is a well-defined parameter by applying barrier thickness, a desired resistance value of the MTJ can be obtained from the choice of a certain barrier thickness. For example, AR is about 1 $k\Omega\mu m^2$ for the MTJ with 9 Å of Al layer for a tunnel barrier that is a thickness limit to control MR without performance degradation in a usual Al sputtering and plasma oxidation process.

The NMOS transistors whose channel resistance is in the range between 200 Ω to 2000 Ω were chosen among

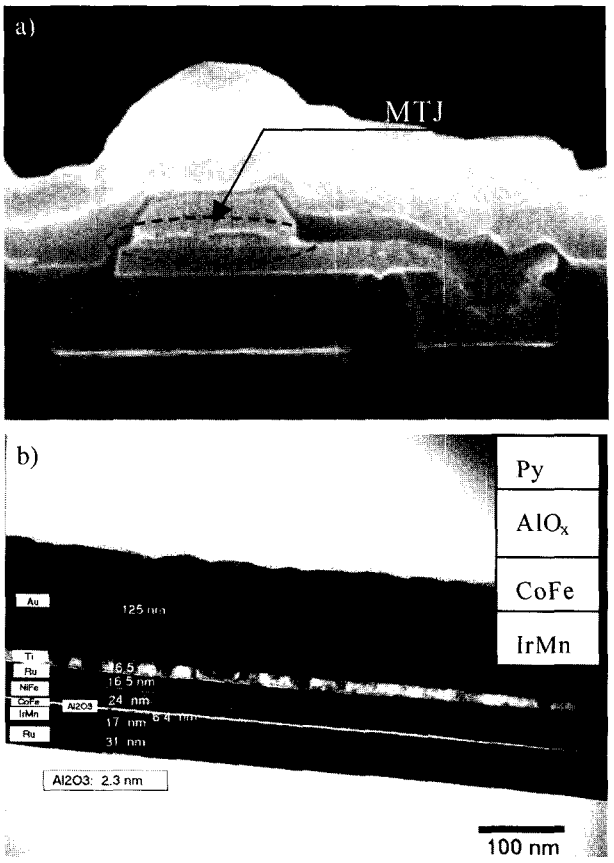

Fig. 1. (a) SEM image of MTJ and (b) TEM Image of multilayer stack for MTJ.

many different sizes by consideration of the MTJ resistance. In general sense, less resistance of core cell is desired for operational speed of actual device. However, the MOS transistor itself has resistance and this resistance becomes a factor of MR drop. So the MTJ resistance

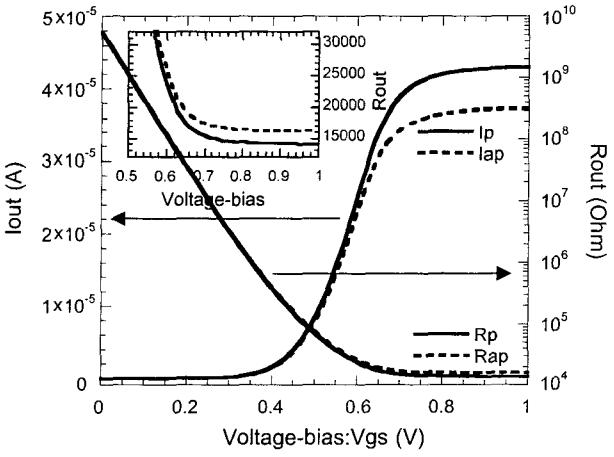

Fig. 2. I_{gs}-V_{ds} characteristics of the MRAM core cell where the MTJ resistance is large enough than the MOS transistor. Insert indicates resistance after the threshold voltage.

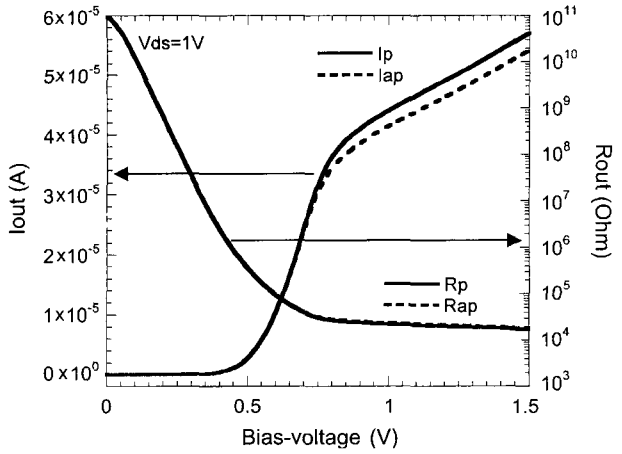

Fig. 3. I_{gs}-V_{ds} characteristics of the MRAM core cell where the MOS resistance is not negligible for the core cell after the threshold voltage.

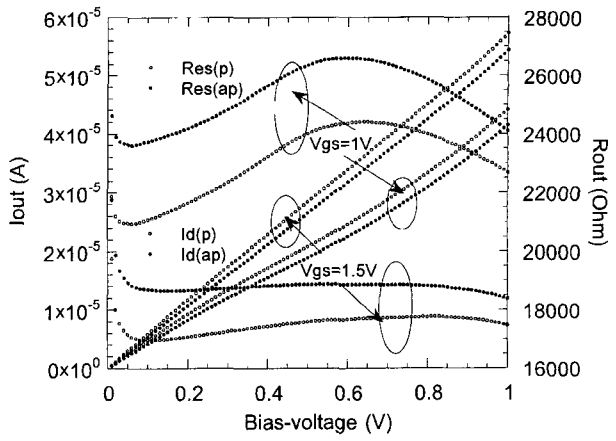

Fig. 4. *I-V* Characteristics of the MRAM core cell.

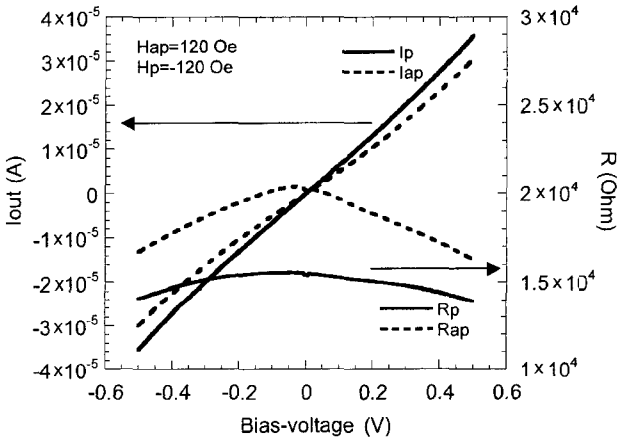

Fig. 5. Bias dependence of MR.

should be chosen for significantly large value where the contribution of the MOS is negligible. Figure 2 shows that I_{gs}-V_{ds} characteristics of the MRAM core cell where the MTJ resistance is large enough than the MOS transistor. The most of resistance attributes to the MTJ after the threshold voltage (0.8 V). The MOSFET size was $W/L = 80\ \mu m/0.16\ \mu m$. The output current or resistance is separated by the applying magnetic field that generates parallel (for $H_{ex} = 120$ Oe) and antiparallel state (for $H_{ex} = -120$ Oe). Figure 3 shows that I_{gs}-V_{ds} characteristics of the MRAM core cell where the MOS resistance is not negligible for the core cell after the threshold voltage. The MOSFET size, $W/L = 0.8\ \mu m/0.2\ \mu m$, is more realistic for the actual core cell layout, however the narrow width induces higher channel resistance and encroaches MR on the core cell.

3. Data Reading

Simple architecture for data reading is attributed to a key role for density consideration. The critical factors for this issue are high MR, uniform resistance over the entire core cell arrays, and appropriate resistance tuning between the MOS transistor and the MTJ.

Once MTJ structure and size are fixed by processing consideration, the dominant effects for maintaining high MR are MR bias dependence and appropriate choice of cell operation condition.

The I-V characteristics for core cell are shown in Fig. 4 where the size of the MOS transistor is $W/L = 0.8/0.2\ \mu m$. The tested core cell shows MR drop by bias dependence becomes to dominate over 0.6 Volt. An estimation of direct margin for data sensing will be estimated by a difference in output current or resistance between parallel and antiparallel state.

The origin of bias dependence on resistance is an inherent property of tunnel barrier. As shown in Fig. 5, the slop of resistance decrease differs from magnetization parallel and anti-parallel state. This difference decreases with applying bias.

The most critical issue will be resistance control for each MTJ over the entire wafer. Either small variation of barrier thickness or area of the MTJ during patterning process makes margin narrower or even destroys resistance boundaries between magnetization parallel and antiparallel state. We point out that issues of process capability are much more important than technology fundamental.

4. Data Writing

The main issues for writing scheme are to find a method for low current operation. This operation requires

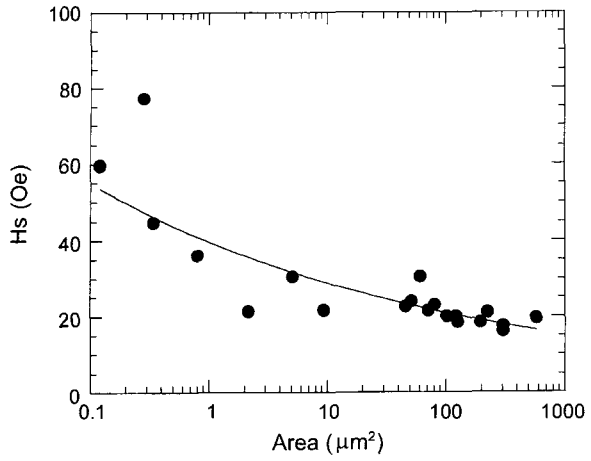

Fig. 6. Size effect for switching field (switching field measured along the exchange bias pinning direction).

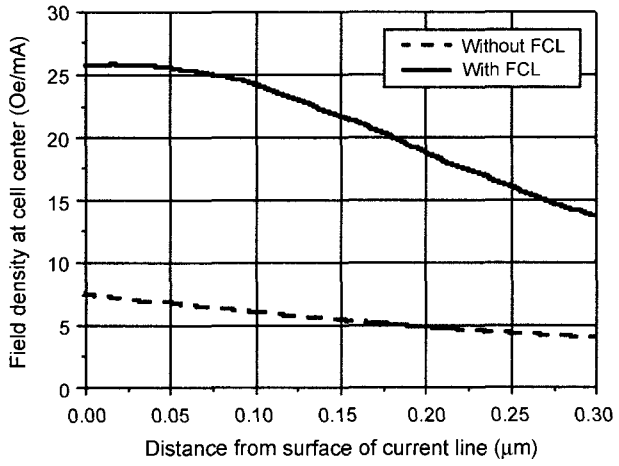

Fig. 7. Estimation of field generation by applying current (with assumption of uniform current density).

reduction of switching field and high field generation by relatively small applying current. Unlike situation of data reading, size effect dominates for magnetization reversal. Hence switching is a major factor to limit device size. Figure 6 shows switching field increase as the MTJ size goes to smaller. It is very important to figure out a magnetic field generated by the writing current. Figure 7 shows a numerical estimation of magnetic field generated by line current with an assumption of uniform current density in the write line. If switching field is 50 Oe and digit line distance from MTJ is 1000 Å, current needs ~8 mA for normal write line. If we apply some special technique such as a Field Cladding Layer (FCL) to write line, ~2 mA is enough for writing data. Those values could be in the acceptable range to 0.1 μm^2 of the MTJ area that is correspond to ~G-bit density MRAM

Actual operation of MRAM uses two directional writ-

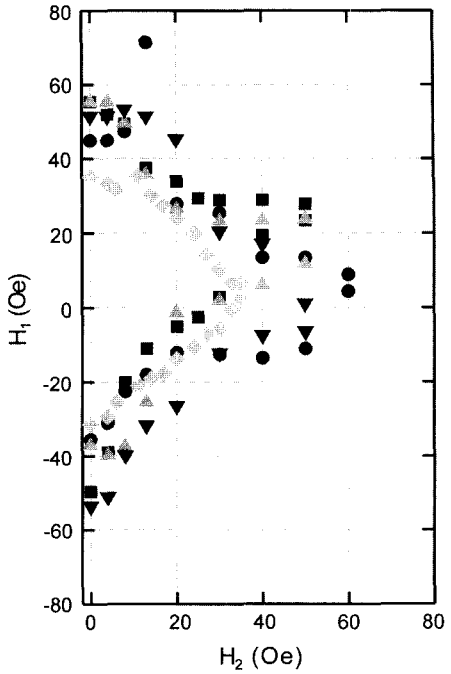

Fig. 8. Asteroid curve for the MTJ: Area = 0.34 μm^2 and elliptical shape. (a write current is measured as H_1 = 35 Oe, H_2 = 30 Oe for example).

ing fields to select a unit cell from two-dimensional core cell array (Fig. 8). One is along the exchange bias pinning direction and the other is perpendicular to the pinning direction. Use of two-directional field makes an advantage to reduce writing field since any points outside asteroid curve can be a choice of writing condition. Another issue related to switching is cell selectivity that is originated from rather fundamental phenomenon such as vortex formation and edge pinning to prevent uniform alignment of magnetic moments. Figure 9-(a) shows a MR curve resulted by this issue. We can easily find this type of distortion in MR curve for small size MTJ samples. If there is kink in MR response curve, a single direction current will select an undesired cell and its magnetization of free layer can be switched statistically. It will result selection fail. Fortunately, data indicate that an appropriate choice of MTJ shape and aspect ratio can reduce distortion of uniform alignment of magnetic moments as shown in Fig. 9-(b). Tested sample is an ellipse with its size 0.12 μm^2, aspect ratio 3.

5. Conclusion

The purpose of this study is to test the fundamental of the technology limit for an actual memory device. Research scope was restricted to only core cell at this stage. After success demonstration of integration process

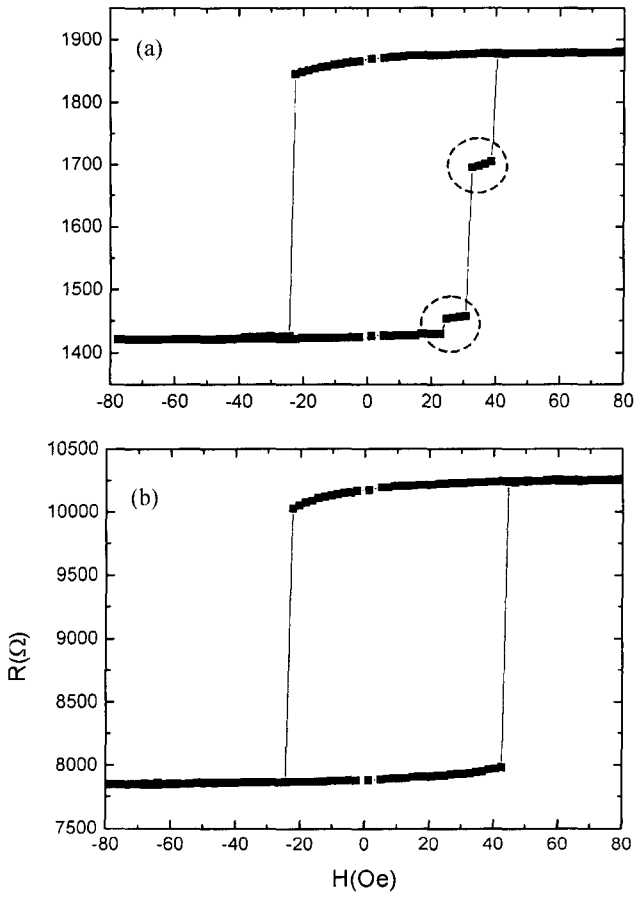

Fig. 9. MR curve of the MTJ samples (a) with local magnetization distortion (size: 0.8 μm^2, shape: ellipse, aspect ratio: 2), (b) without local magnetization distortion (size: 0.12 μm^2, shape: ellipse, aspect ratio: 3).

of MTJ and MOS transistor as a core cell unit, our facilities are ready to test the MRAM technology.

The key issues of MRAM technology as a future memory candidate are resistance control and low current operation for small enough device size. Resistance seems to be irrelevant to the size effect. MR is limited by the barrier thickness. Switching issues are controllable with a choice of appropriate shape and fine patterning process. Presenting data meet fundamental requirement to satisfy the condition for coding/decoding function down to 0.1 μm^2 MTJ size that is a corresponding size to ~G-bit density capability. Finally it should be pointed out that controls of fabrication is rather important to realize an actual memory device for MRAM technology.

Acknowledgements

Author thanks Dr. K. J. Lee for sharing his simulation works and valuable discussion about the general topics of magnetic switching.

References

[1] M. Baibich, J. Broto, A. Fert, F. Nguyen Van Dau, F. Petroff, P. Etienne, G. Creuzet, A. Friederich, and J. Chazelas, "Giant magnetoresistance of (001)Fe/(001)Cr magnetic superlattices", Phys. Rev. Lett. **61**, 2472-2475 (1988).

[2] R. R. Katti, "Current-in-plane pseudo spin valve device performance for giant magneto-resistance random access memory application", J. Appl. Phys. **91**, 10, 7245-7250 (2002).

[3] R. E. Scheuerlein, W. J. Gallagher, S. S. P. Parkin, C. A. Lee, S. T. Roy, R. Robertazzi, and W. R. Reohr, "A 10ns read and write non-volatile memory array using a magnetic tunnel junction and FET switch in each cell", ISSCC Digest of Technical Papers **43**, 128-129 (2000).

[4] P. K. Naji, M. Durlam, S. Tehrani, J. Calder, and M. F. DeHerrera, "A 256 kb 3.0 V 1T1MTJ nonvolatile magetresistive RAM", ISSCC Digest of Technical Papers **44**, 122-123 (2001).