ISSN (Print) 1226-1750
ISSN (Online) 2233-6656
Journal of Magnetics 25(2), 150-156 (2020) https://doi.org/10.4283/JMAG.2020.25.2.150

Optimizing the Geometry of Chiral Magnetic Logic Devices

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(Received 14 May 2020, Received in final form 16 June 2020, Accepted 16 June 2020)

We investigated how geometry affects chiral magnetic logic devices, using micro-magnetic simulation. The logical NOT gate in the device was operated by current-induced domain wall (DW) motion in perpendicularly magnetized nanowires with a locally modulated in-plane magnetic anisotropy (IMA) region, where the up-down DW is switched into a down-up DW by current. We modulated the width of the nanowires as well as the length of the IMA region and found that an optimized geometry exists which depends on the Dzyaloshinskii-Moriya Interaction. Integrating the optimized NOT-gate, we then demonstrated NAND or NOR logic operations. Our results provide design guidelines for the magnetic logic device, paving the way to functional magnetic logic-in-memory devices.

Keywords : magnetic domain wall, magnetic logic, chiral magnetism

1. Introduction

Recent achievements in data science, especially in machine learning and artificial intelligence, have enabled intensive research in various fields [1-4]. In many of those fields, it is necessary to deal with large raw data sets, making frequent access to data storage inevitable. However, the conventional architectures of computer systems have an intrinsic speed dilation called the 'Von Neumann bottleneck' [5]. The bottleneck is a consequence of slow memory access time compared to relatively fast data processing, produced by the physical separation of the processing unit and memory. One possible solution to overcome the Von Neumann bottleneck would be to put memory in the processing unit, the so called 'Process in Memory (PiM)' architecture.

Many computing devices now use magnetic memory devices such as hard-disk drives (HDD), to store information. In an HDD, the data are stored in the direction of magnetization of a magnetic domain, either up or down, and the data are accessed by the mechanical rotation of a platter. However, the energy consumed by this mechanical rotation has become an increasingly important problem. To reduce energy consumption, a novel type of magnetic memory, so called 'racetrack memory' has been proposed [6]. In this memory, the mechanical rotation is replaced by current-induced domain wall (DW) motion, and this can significantly improve the amount of power consumed as well as overall mechanical stability, compared to a conventional HDD. However, to put this new memory into a processing unit, it will be necessary to develop a logic device that also uses current-induced DW motion.

A decade ago, magnetic logic devices were developed that used DW motion [7]. For DW manipulation, however, those devices relied on an external magnetic field with a complicated device structure, which limits practical applications. Later, a spin torque majority gate, which uses current-induced DW motion in a cross-shaped structure, was proposed [8], but the experimental realization has not been achieved yet. Very recently, current-driven chiral magnetic DW logic devices have been experimentally demonstrated [9]. In this device, the logic operation is achieved by using the chiral DW formation, which is physically rooted in an antisymmetric exchange interaction called the Dzyaloshinskii-Moriya Interaction (DMI). A locally modulated in-plane magnetization region is necessary for logic operation. However, understanding of the physical mechanism behind the logic operation as well as the effect of geometric variation has remained elusive.

In this work, we investigate the effect of geometry on the operation of a chiral magnetic NOT gate, using micro-magnetic simulation. For this purpose, we modulated the width of the nanowire and the length of the in-plane magnetic anisotropy (IMA) region, and checked whether the

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logic operated successfully without errors.

We found that the logic operation is only possible for specific geometries, and the geometrical constraint is closely related to the strength of the DMI. Furthermore, we demonstrate that it is possible to achieve NAND and NOR logic operations by integrating the optimized NOT-gate with a symmetry breaking magnetic field. Our work elucidates the operating mechanism underlying the chiral logic devices, and provides a design guideline for magnetic logic devices, and therefore paves the way for the realization of magnetic logic-in-memory devices.

2. Method

Figure 1(a) shows the device geometry used in our study. We assumed ferromagnet (FM)–non-magnet (NM) bilayer structures with a perpendicular magnetic anisotropy (PMA), of the type that have been typically used in spin-orbit torque (SOT)-driven magnetic DW motion experiments [10-13]. Nanowires of 500-nm-length and variable widths were employed to investigate the DW motion-induced logic operation. We intentionally assigned zero PMA at the center of the nanowire (the green region in Fig. 1(a)), so that the magnetization of the center region pointed in the in-plane direction. As a result, the nanowire was composed of sequential PMA-IMA-PMA regions. Hereafter, we denote the left PMA region as PMA-1 and the right PMA region as PMA-2.

To investigate the DW motion-based logic operation, we developed a custom μ-magnetic simulator by numerically solving the Landau-Liftshitz-Gilbert equation, given by

$$\partial_t \vec{m} = \gamma \vec{m} \times \vec{H}_{eff} + \alpha \vec{m} \times \partial_t \vec{m}, \quad (1)$$

where $\gamma = 2.211 \times 10^5$ m /A·s is a gyromagnetic ratio, α is the Gilbert damping parameter, and $\vec{H}_{ext}$ is the effective magnetic field, defined as follows:

$$\vec{H}_{eff} = \frac{2A}{\mu_0 M_s}\vec{\nabla}^2\vec{m} + \frac{2D}{\mu_0 M_s}\left[\vec{\nabla} m_z - \left(\vec{\nabla}\cdot\vec{m}\right)\hat{z}\right] + \frac{2K_u}{\mu_0 M_s} m_z + \frac{\hbar}{2e}\frac{\theta_{sh} j}{\mu_0 M_s t}\vec{m}\times\vec{\sigma} + \vec{H}_{demag} + \vec{H}_{ext}. \quad (2)$$

Here A is the exchange stiffness, D is the DMI constant, K_u is the uniaxial anisotropy constant, M_s is the saturation magnetization, θ_{sh} is the spin Hall angle of NM, j is the current density flowing along the NM, t is the thickness of FM, $\vec{H}_{demag}$ is the demagnetization field and $\vec{H}_{ext}$ is the external magnetic field. We assumed the materials parameters of Pt/Co bilayer system [14] mimicked the real situation: $A = 1.3 \times 10^{-11}$ J/m, $D = 1.6 \times 10^{-3}$ J/m^2, $K_u = 3 \times 10^5$ J/m^3, $M_s = 5.6 \times 10^5$ A/m, and $\alpha = 0.3$. The Spin Hall angle θ_{sh}, which represents the charge-to-spin conversion efficiency of NM was assumed to be 0.1 [15-17]. The total simulation region was set to be 500 nm × 60 nm × 0.6 nm, and the rectangular unit cell size was 2 nm × 2 nm × 0.6 nm. Total simulation time was 2.5 ns with a time step of 2 fs to numerically solve the Landau-Liftshitz-Gilbert equation. Note that magneto-crystalline exchange length ($\sqrt{A/K_u}$) is 6.6 nm and magneto-static exchange length ($\sqrt{2A/\mu_0 M_s^2}$) is 8.1 nm, hence size of rectangular unit cell is proper for micro-magnetic simulation.

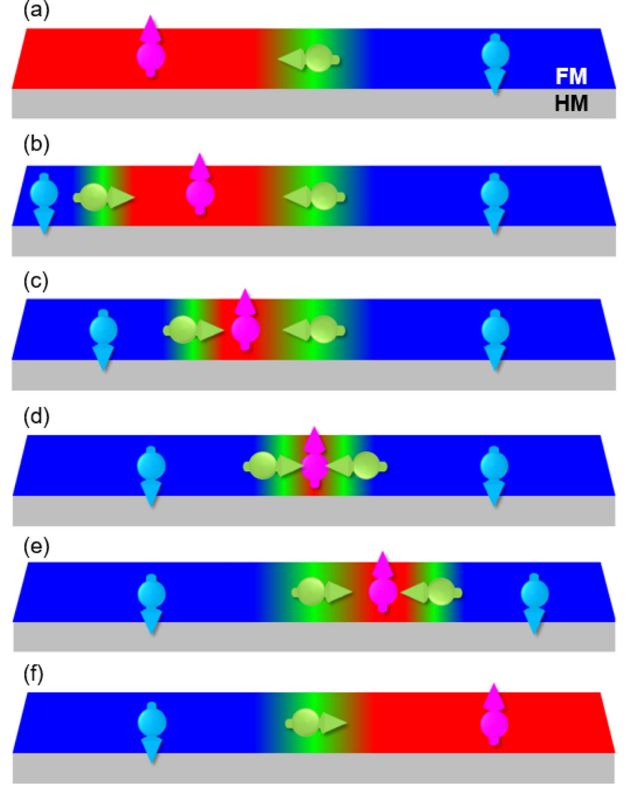

Fig. 1. (Color online) Device geometry and concept of domain wall-based NOT-gate operation. FM-HM bilayer is employed. Red and blue regions correspond to the up and down magnetization, and the green region is the area having in-plane magnetic configuration. Note that center of wire has in-plane magnetic anisotropy. (a)-(f) Schematic illustration of NOT-gate operation. (a) Initial magnetization configuration. The DMI originating from FM-NM interface stabilizes the chiral spin configuration (up-left-down). (b) Chiral DW (narrow green region at the left of wire) is injected from the left edge and moved to the right by current-induced spin orbit torque. (c)-(e) Magnetization switching induced by the current-induced DW motion along the nanowire. (f) Magnetization configuration of final state after the DW motion.

3. Results

3.1. NOT gate operation

Figures 1(a)-1(f) show a schematic illustration of the DW motion-based NOT-gate operation [9]. Initially we assumed up and down magnetization in PMA-1 and PMA-2, respectively. Because of the DMI [10-12], the magnetization direction of the IMA region was determined to be left, so the magnetization configuration of the nanowire can be "up (PMA-1) – left (IMA) – down (PMA-2)" as shown in Fig. 1(a). This can be considered an "effective DW" because the magnetization configuration along the nanowire is the same as DW.

However, there is a clear difference between the "effective DW" and real DW, in that the "effective DW" is fixed at the IMA region and cannot move. We then created a DW at the left edge of the nanowire and pushed it by applying an electric current along the $+x$ direction (Fig. 1(b)). The spin Hall effect of NM generates a transverse spin current (whose magnetic moment aligns along the $-y$ direction), and this spin current exerts torques to the DW in the neighboring FM layer. This so-called spin orbit torque (SOT) drives the DW to the right direction. When the DW arrives near the IMA region (Fig. 1(c)), it pushes the "effective DW" since the DW and effective DW form homochiral spin configurations, that is, "down-right-up-left-down", which is energetically stabilized by DMI. As the DW is moved to the right by the SOT, the "effective DW" is pushed out to the right, and finally the "effective DW" escapes from the IMA region and moves to the right end of the nanowire (Fig. 1(e)). The original DW is then absorbed in the IMA region and forms a "down (PMA-1) – right (IMA) – up (PMA-2)" magnetization configuration (Fig. 1(f)), which is the reverse of the state in the initial configuration. Accordingly, the current-induced DW motion along (PMA-1) – (IMA) – (PMA-2) nanowire switches the magnetization state from up-left-down to down-right-up, which corresponds to the NOT logic operation.

Figures 2(a)-2(g) show the simulation results for the DW motion-based NOT-gate operation. As we expected, the current-induced DW motion causes magnetization switching of the nanowire from up-left-down to down-right-up. We also checked the NOT logic operation for the opposite polarity, i.e., with an initially down-right-up state. As shown in Figs. 2(h)-2(n), the logic operation is reproduced for the opposite polarity, which indicates that the logic operation is irrespective of the initial magnetization direction. This suggests that the proposed NOT gate operates properly no matter what the initial state is. We note that the DW tilting during its motion was induced by the DMI [19-21].

3.2. Phase diagram for NOT gate operation

The operation of the NOT gate can depend on magnetic properties as well as the geometry of the device. We investigated the effects of geometry and DMI, which is crucial for the logic operation. Since the IMA region is crucial for the logic operation, we investigated the IMA region's optimum length as a function of wire width and DMI. Figure 3(a) shows the phase diagram of the NOT logic operation for various IMA lengths (l) and nanowire

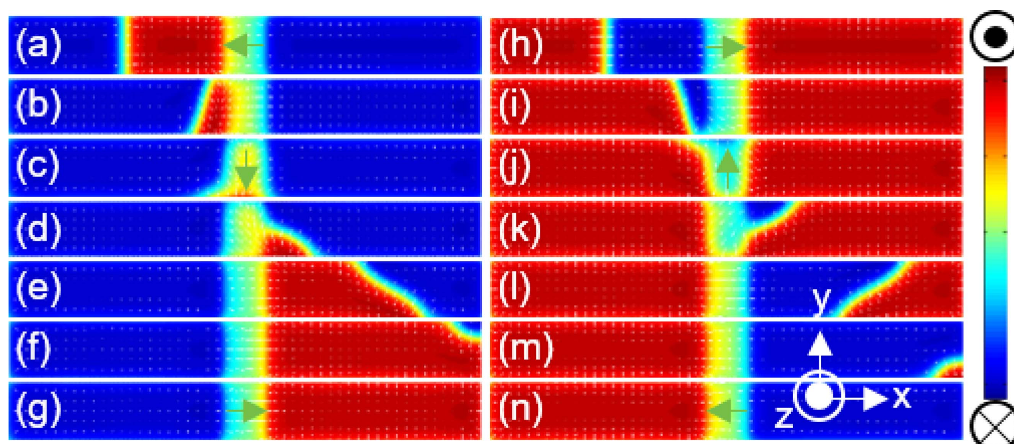

Fig. 2. (Color online) μ-magnetic simulation of NOT gate. Red and blue regions represent the up and down magnetization direction. The green color represents the in-plane magnetization. (a)-(g) DW motion-induced switching process from up-down configuration to down-up configuration. (h)-(n) DW motion-induced switching process from down-up configuration to up-down configuration. Time interval between each figure is 0.4 ns for both (a)-(g) and (h)-(n). The length and width of nanowire are 500 nm and 60 nm, respectively. The length of in-plane region (green area at the center of nanowire) is 50 nm. Current density of 4.9×10^{11} A /m^2 was used for DW motion.

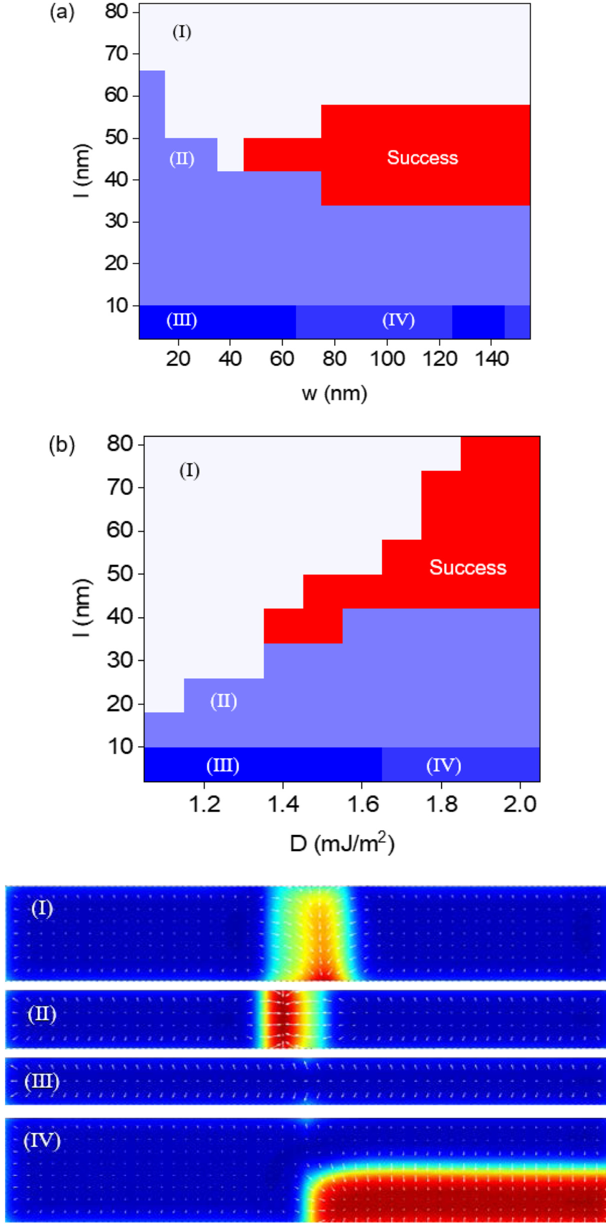

Fig. 3. (Color online) (a) The phase diagram of NOT gate operation under current density $j = 4.9 \times 10^{11}$ A/m^2, D = 1.6 mJ/m^2. l is length of IMA region, and w is width of magnetic nanowire. (b) The phase diagram of NOT gate operation under current density $j = 4.9 \times 10^{11}$ A/m^2, $l = 60$ nm. (I)-(IV) Failed results of μ-magnetic simulation after 4 ns.

widths (w). We found that the NOT logic operation was possible only in the red colored regime, which means that an optimum geometry exists for the NOT gate operation.

Figure 3(b) shows the phase diagram of the NOT logic operation for various IMA lengths (l) and DMI strengths (D). Again, there is an optimum range of IMA length depending on DMI. The results in Figs. 3(a) and 3(b) suggest that we should carefully design the geometry and material parameters to obtain the NOT logic gate. To further understand the mechanism underlying the NOT logic, we looked closely at the simulation results and found that the failed logic operations can be divided into several cases, as shown in Fig. 3(c) (we give each case a different color in Fig. 3(a) and 3(b)). Case I in Fig. 3(c) appears when the IMA length is very large. In this case, the up domain is found to be confined in the IMA region. On the other hand, Case II in Fig. 3(c) appears for narrow IMA length, where the up domain of the PMA-1 cannot enter into the IMA region. When the IMA length becomes very small, then the DW either disappears (case III in Fig. 3(c)) or becomes pinned (case IV in Fig. 3(c)) in the IMA region.

3.3. Underlying mechanism of NOT gate operation

To understand the phase diagrams in Figs. 3(a) and 3(b), we considered each DW propagation step shown in Fig. 1. The DW created at the left edge of the wire is propagated to the right by the SOT (i.e., the process from Fig. 1(b) to Fig. 1(c)). In this case, one can consider that the SOT-induced effective field ($\vec{H}_{SOT}$) drives the DW. When the DW arrives near the IMA region (Fig. 1(c)), the $\vec{H}_{SOT}$ competes with the DMI-induced effective field $\vec{H}_{DMI}$ [12]. The strength of the DMI field $\vec{H}_{DMI}$ originating from the IMA region can be described by the effective magnetic field originating from the DMI. If the polar angle of spin changes uniformly from 0 to π under length Δ along x-direction, then the effective magnetic field due to the DMI at polar angle $\pi/2$ is given by

$$\vec{H}_{DMI}\Big|_{\theta=\pi/2} = \frac{2\pi D}{\mu_0 M_s \Delta}(-\hat{x}), \tag{3}$$

which can be derived from Eq. (2). If the strength of $\vec{H}_{SOT}$ is smaller than that of $\vec{H}_{DMI}$, the DW cannot enter into the IMA region as shown in case II in Fig. 3(c). Since the $\vec{H}_{DMI}$ is proportional to D/l, case II appears for small l or large D, which explain the phase II regime in Figs. 3(a) and 3(b).

If we reduce the $\vec{H}_{DMI}$ by increasing l or by decreasing D, then the DW can enter into the IMA region as shown in Fig. 1(d). When the DW enters into the IMA region, it does not maintain its structure due to the absence of PMA. Since the thickness of the ferromagnet is much less than the width or length of the device, the magneto-static interaction prefers an in-plane Néel type DW, which is typically quoted as 'transverse DW' [18]. In this case, the magnetization rotates in xy plane and thus, the center of DW lies along y direction. On the other hand, the DMI prefers an in-plane Bloch type DW, in which the magnetization rotates in xz plane and the center of DW points

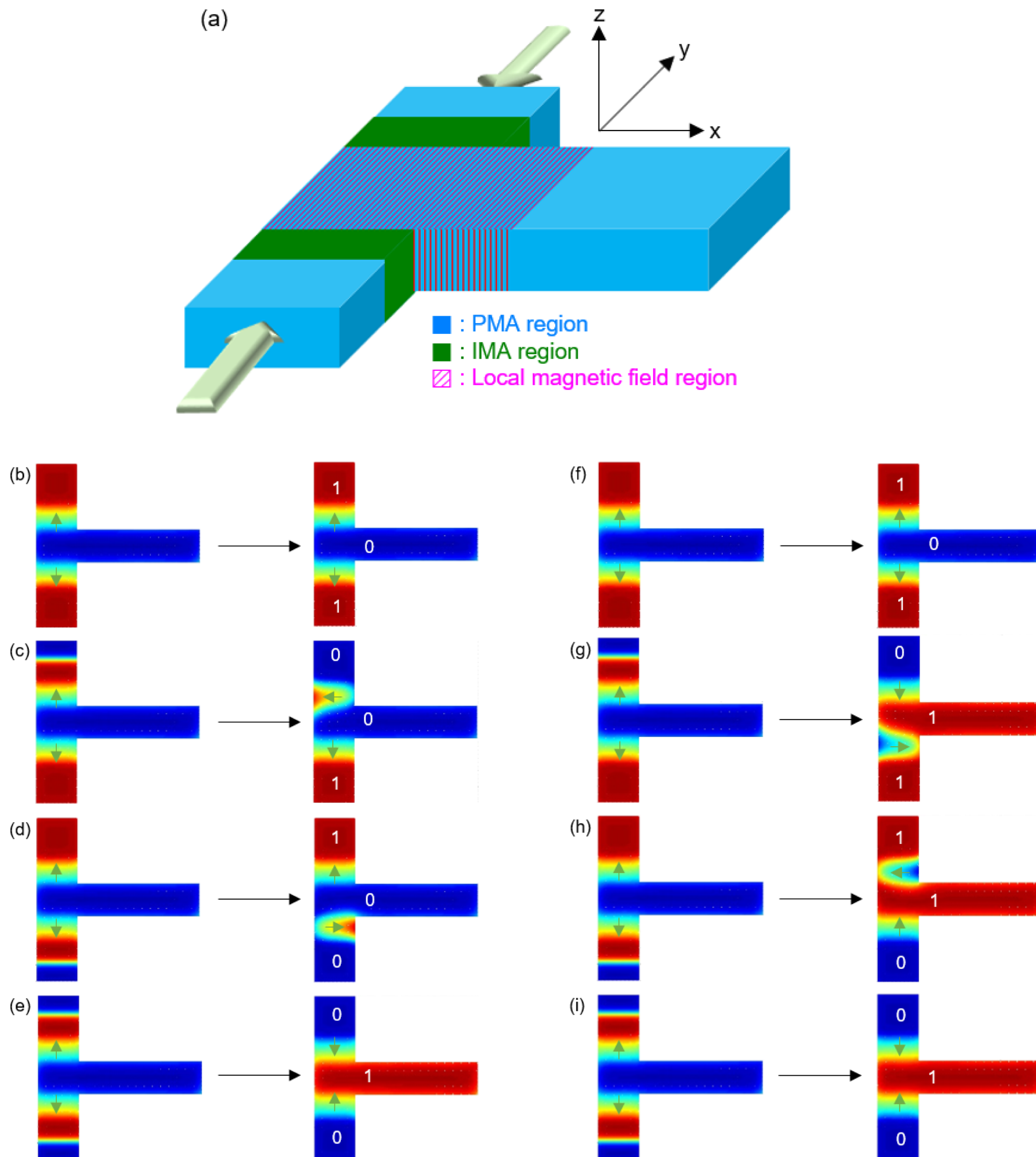

Fig. 4. (Color online) (a) Schematic illustration of NAND or NOR logic devices. The width and length of input branch are set to be 50 nm and 80 nm, respectively. The length of output branch is 200 nm. Cyan color represents PMA region, green color represents IMA region. Local magnetic field is applied in the shaded region to break the symmetry at central region. (b)-(e) Results of NOR logic operation. (b) 00 → 1, (c) 10 → 1, (d) 01 → 1, (e) 11 → 0. (f)-(i) Results of NAND logic operation. (f) 00 → 1, (g) 10 → 0, (h) 01 → 0, (i) 00 1. For (b)-(i), all left figures are initial states, and all right figures are final states. The current pulse of 0.7-ns-duration and 3-ns-period are applied two times. The current density for each input branch is 1.6×10^{12} A/m^2.

along *z* direction. Therefore, the competition between magneto-static interaction and DMI leads the intermediate DW state of which center magnetization points in-between *y* and *z* axis. When the effective DMI field is small, the DW is close to an in-plane Néel wall which is immune to the spin Hall effect-induced SOT. On the other hand, if the effective DMI field is sufficiently large, then the DW is getting closer to the in-plane Bloch wall so that SOT will translate the in-plane DW, even in the IMA region. From Eq. (3), the effective DMI field is enhanced when the length of the IMA region is short or the DMI strength is high, therefore, a logical NOT operation is possible in this regime.

Cases III and IV in Fig. 3(c) show improper NOT-gate operations when the IMA region is very narrow. When the IMA region is very narrow, we can consider it to be a

pinning site [19]. In this case, the pinning strength depends on the DMI. Thus, the DW can be either pinned (case IV) or depinned (case III) depending on the strength of the DMI. The asymmetric DW pinning in case IV is the result of the dynamical tilting of the DW [20-22] which generally occurs in wider nanowires. These considerations can explain phases III and IV in Figs. 3(a) and 3(b).

3.4. Operation of NAND and NOR gate

The NAND or NOR logic operations are known as the fundamental building blocks of a complete logic operation, because a single NAND (or NOR) operation can build a complete Boolean algebra [23]. The NAND or NOR gate can be formed by integrating two NOT-gates. Figure 4(a) shows a schematic illustration of the NAND or NOR devices. The device is composed of two NOT gates as the upper and lower input branches, and one output branch. We intentionally created an IMA region on each input branch. Electric current flows along the $-y$ ($+y$) direction in the upper (lower) branch, and is ejected along the $+x$ direction at the output branch. In an ohmic material the current density distribution at the center of the two input branches is calculated by numerically solving the Laplace equation. All of the magnetic parameters are the same as those used in the NOT-gate.

When we flow current along the device, each input branch acts as a NOT gate, as we demonstrated in the previous section. However, the magnetization direction at the center of the device is not well defined because it is impossible to form a homo-chiral magnetic texture along the y-direction. To break the symmetry, we applied a magnetic field (H_B) in the perpendicular direction in the shaded region of Fig. 4(a). Figures 4(b)-4(e) show the logic operation for $\mu_0 H_B$ = +15 mT. It is clear that the results demonstrate the NOR gate operation. Figures 4(f)-4(i) show the NAND operation, which was obtained by applying $\mu_0 H_B$ = −15 mT. Therefore, one can easily obtain reconfigurable NAND or NOR gates by controlling the symmetry breaking field.

4. Discussions

As we discussed in the previous section, the logic devices operate within a specific range of IMA geometry and DMI. Therefore, modulating the anisotropy of a local area and achieving high DMI is crucial to realize the device. It is well-known that magnetic anisotropy can be controlled by local oxidation [9, 24, 25] or local ion irradiation [26-28]. The optimization of DMI is also feasible, because magnetic thin films having DMI strength have been used, as in Fig. 3(b) [29, 30]. As for the NAND and NOR logic gates, it is necessary to apply an additional magnetic field to break the symmetry. This additional magnetic field can be achieved by interlayer exchange coupling [31, 32] or antiferromagnetic exchange bias [33]. One can also utilize a stray field by placing a nanomagnet near the intersection region of the NAND or NOR logic gate.

Power consumption is another crucial issue in logic devices. We calculated the dynamic power consumption of the magnetic NOT gate shown in Fig. 2. By considering the operation time of 1 ns and heavy metal (Pt) conductivity, the energy consumption was estimated to be 3.82 fJ. This value is not much smaller than that of CMOS logic devices [34]. However, the magnetic nature of our logic devices provides other advantages: the magnetic logic is non-volatile, and thus a significant reduction in static power consumption is expected. The power consumption can be further reduced by using highly efficient spin sources [35-39].

5. Conclusion

In conclusion, we studied magnetic domain wall-based logic devices using a custom-built μ-magnetic simulator. The combination of DMI and locally modified PMA evoked a chiral coupling between the up and down domains. The current-driven SOT induced sequential switching of the input and output bit, which enables the NOT gate operation. By integrating the NOT gates with a symmetry breaking field, we successfully demonstrated more complicated logics such as NAND and NOR gates. We also studied the effect of device geometry as well as magnetic parameters, and determined that an optimized geometry exists, which depends on the strength of the DMI. We discussed the mechanism underlying the logic operation. Our results provide design guidelines for the magnetic logic device, and therefore pave the way for the realization of magnetic logic-in-memory devices.

Acknowledgments

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea Government (No. 2019M3F3A1A02072477).

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