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Multichannel FPGA-based Data Acquisition System for Fan-beam Dual Energy X-ray Absorptiometry

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This study aimed to develop a multichannel field programmable gate array (FPGA) based data acquisition (DAQ) system that could process 8 analog signals from a 1 × 8 LYSO array coupled with a Geiger-mode avalanche photodiode (GAPD) for fan-beam dual-energy X-ray absorptiometry (DEXA) system. Each analog input signal was digitized using an 8-channel analog-to-digital converter (ADC) with a 125 MHz sampling rate and an input range of -1.0 to 1.0 V. The 14-bit digital signals were then fed into a Xilinx Virtex-6 FPGA-based evaluation board that implemented digital signal processing logic. The collected low- and high-energy events of each pixel for each input channel were stored in an on-chip block ram-based first-in-first-out (FIFO) module, and then further transmitted to a personal computer (PC) via the USB port. The intrinsic characteristics, spectral responses, and image acquisition were performed. The estimated coefficient of determination (R^2) was 0.999 in voltage linearity and no considerable alterations in voltage resolution were observed. The energy resolutions of the peak 59.5 keV (Am-241) were ~28.2 %. Dual-energy peaks were isolated in the X-ray energy spectra. The synchronization between the movement part of the DEXA system and the timing control block inside the FPGA chip was well controlled in various conditions. The DEXA phantom images for each pixel were clearly resolved. This study demonstrated that FPGA with only on-chip memory resources can be used to build a multichannel DAQ system for fan-beam DEXA systems.

Keywords : Field programmable gate array (FPGA), data acquisition system (DAQ), Dual Energy X-ray Absorptiometry (DEXA), non-magnetic LYSO-GAPD detector

1. Introduction

Dual energy X-ray absorptiometry (DEXA) is one of the most widely used techniques for examining the condition of bones. In addition, the technique exhibits excellent performance in diagnosing osteoporosis and determining fracture risk and is suitable for measuring bone mineral density (BMD) [1-3]. For these reasons, DEXA has become one of the most researched medical imaging topics. Within this field, data acquisition (DAQ) systems play an important role in controlling, processing, and summarizing the performance of the whole instrumentation. The advantages of field programmable gate array (FPGA)-based DAQ systems in the medical imaging instrumentation area have been demonstrated in previous research [4-10]. Compared to application specific integrated circuit (ASIC) chips, the flexibility and time-to-market characterization of these systems have made a significant contribution to optimizing system performance. Conventional general-purpose DAQ systems for multichannel radiation signals in the medical imaging field are built with large memory resources and incur exorbitant costs, limiting the scalability in practical applications. This problem becomes more serious as the number of channels increases. To address this issue, many previous efforts have attempted to process raw radiation events online instead of storing all events, complete with their energy and coarse time information. A typical example here is the coincidence module in positron emission tomography-magnetic resonance imaging (PET-MRI) [7, 11, 12]. Moreover, the limitation of the number of I/O pins renders the design of an FPGA-based system for multichannel signals processing.

Cadmium-zinc-telluride (CZT) or cadmium telluride

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(CdTe) have been considered a representative detector for DEXA implementation due to its good stopping power, excellent energy resolution, room temperature operation, and well-established techniques. However, these compound semiconductor detectors have a number of features that may render their prolonged implementation difficult. They are susceptible to irradiation damage, incomplete carrier collection, and a large dark current. Their high price and fragile structure also limit their applicability. As an alternative, LYSO-GAPD DEXA detector, which combine high-performance scintillation crystals with a compact photosensor, was recently reported [13-16]. This X-ray diagnostic detector has several potential merits including a relatively high count-rate owing to its fast decay time and small crystal volume due to its good stopping power. In addition, they could be potentially affordable and cost-effective because of the availability of suppliers for the components, enabling mass production. A previous study verified that LYSO-GAPD DEXA detector could provide the moderate energy resolution to distinguish the low- and high-energy-band from the incident dual-energy X-ray, and clearly resolved DEXA images with comparable qualities were acquired by using various BMD phantoms. On the other hand, the scope of our previous study was limited to the performance characterization of the pencil-beam DEXA scanner that used single channel LYSO-GAPD detector to acquire DEXA image.

This paper presents the design of an FPGA-based DAQ system, using the FPGA chip's memory resources for the 8 channels of a fan-beam DEXA system which has advantages including fast operating time, and low scattering compared with pencil-beam and cone-beam [14]. Furthermore, the potential is explored for controlling 64 channels with only one FPGA chip. This paper is organized as follows. First, the structure of the system is described, followed by the FPGA logic. Then, the intrinsic performance of the DEXA detector module is presented, followed by the image performance.

2. System Structure

2.1. DEXA system configuration

An X-ray source used in this study consisted of an integrated Monoblock system (XRB80; Spellman, Germany). The emitted X-ray beam angle was approximately 75°. The tube voltage was set to 80 kVp, while the tube current was adjusted for each experiment (as explained below). A lead collimator with a 1-mm hole diameter and a 3-mm thickness was installed on the X-ray tube. The cerium sheet (0.1 mm thick) was used as a K-edge filter for generating the effective dual energy peaks of ~30 keV and ~60 keV.

The detector module and X-ray tube were positioned on opposite sides. The source-detector distance (SDD) and source-object distance (SOD) were 630 mm and 200 mm, respectively. The detector module consisted of a 1 × 8 array of lutetium yttrium oxyorthosilicate (LYSO) crystals, each with a dimension of 3 mm × 3 mm × 2 mm, coupled with a Geiger mode avalanche photodiode (GAPD) array with 3 mm × 3 mm pixels, which has exhibited good characteristics in DEXA applications [13-16].

2.2. Analog signal processing unit and digital signal processing unit

The signals from the detector module were driven via a 2 m flexible flat cable (FFC) and then amplified by current feedback charge-sensitive amplifiers using high-gain operational amplifiers before being fed into the analog-to-digital converter (ADC) board having a sampling rate of 125 MHz and an input range of -1.0 to 1.0 V (AD9681, Analog Devices, MA, USA) to digitalize the signal. These digitized signals were then further processed in a Xilinx Virtex-6 FPGA (XC6VLX75T-2FFG784C)-based evaluation board (HSC-ADC-EVALEZ, Analog Devices, MA, USA) (Fig. 2(b)). Data were written to the

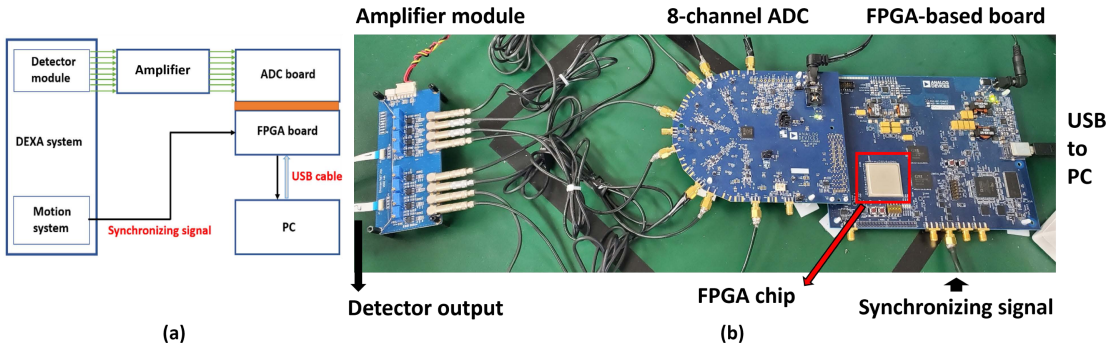

Fig. 1. (Color online) Fan-beam DEXA system. (a) Block diagram. (b) Analog signal processing and digital signal processing.

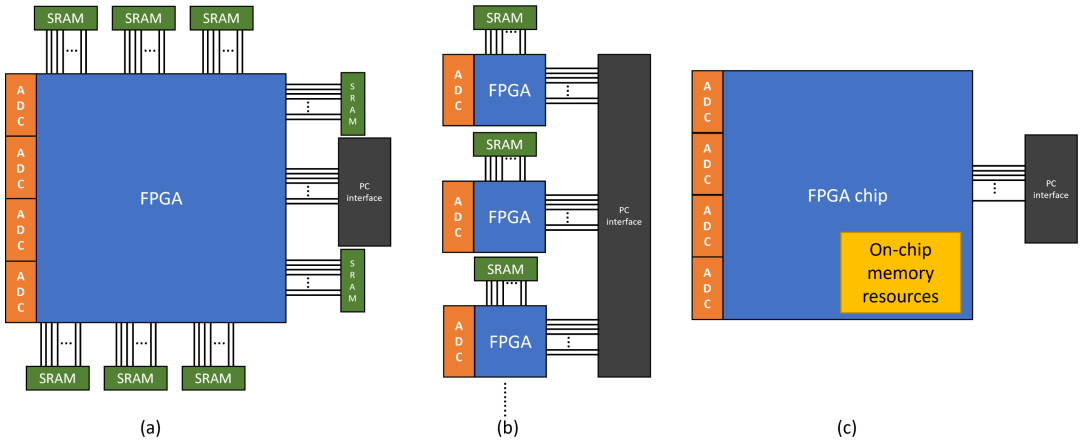

Fig. 2. (Color online) Comparison between general purpose DAQ used for a multichannel medical imaging system with memory component for each channel (a) one FPGA-chip control multiple channels; (b) one FPGA-chip control one channel and (c) proposed design used in this project with only on-chip memory resources.

FPGA on-chip memory resources (block RAM) before being transmitted to a PC via a USB cable. In addition, necessary parameters that are utilized to optimize the performance of DAQ systems (such as cut-off threshold levels, low- and high-energy windows, and synchronization timing for matching with motion parts) could be adjusted in the PC through a serial peripheral interface (SPI). The DAQ system was operated at room temperature without any cooling system.

3. FPGA Logic Synthesis

In this system, FPGA logic should be responsible for all digital processing, in both the engineering mode (for evaluating the intrinsic performance of the DAQ system) and scanning mode (for characterizing the image performance). This FPGA project was designed to store a maximum of 32768 16-bit data for each input channel (575.6/702 Kbyte-82 % on-chip memory resources). Table 1 summarized some typical resources used for this design from ISE 14.7 software (Xilinx, San Jose, California, USA), which was used for the logic implementations and circuit synthesis. The number of slice registers and the number of slices LUTS, which demonstrate the ability of FPGA in parallelism logic processing, were insignificant compared with its ability. The Number of bonded IOBs which shows the number of pins as input and output is half of its quantity including 16 pins for a differential input signal of 8 channels and the rest for controlling the signal and communicating with the PC.

3.1. Engineering mode

The energy of the radiation event could be defined by the voltage amplitude. The analog signals were fed into

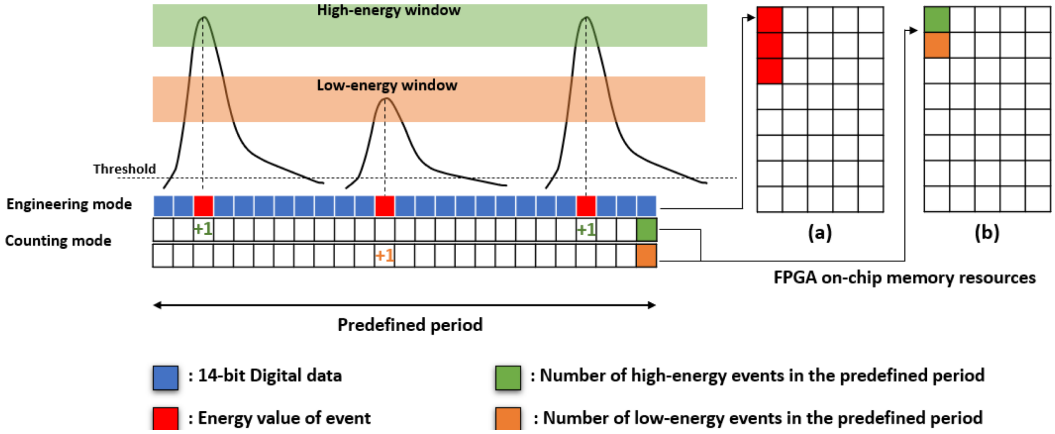

Fig. 3. (Color online) Processing of (a) Engineering mode which stores 16-bit (14-bit ADC and two 0 at LSB) energy value of each event and (b) Counting mode which stores the number of events in the predefined period.

the ADC parts, and then these digitized signals were further processed in the FPGA block.

Whenever a digital signal appears with a value larger than the threshold level, the FPGA block decides the next ~60 ns (longer than the ~45 ns rising edge of the event pulse) belongs to the event pulses, then finds the maximum value in that period and writes it to the on-chip block RAM-based first-in-first-out (FIFO). Then, the next ~450 ns falling edge period is skipped.

In the engineering mode, the block of data is transmitted to the PC when the memory is full and is then ready for the next processing cycle. Therefore, the experiment was not continuous. Instead, there was a time gap between each processing cycle, which depended on the speed of the PC. This issue occurs with increasing the tube current because the memory will be full faster (Fig. 3(a)). Therefore, the DAQ system would require a higher data transmission rate to the PC affecting significantly the continuity of the experiment. The engineering mode with the basic raw data of energy and a coarse time for each event could not complete the DEXA's target.

3.2. Counting mode

In the fan-beam DEXA system, channel quantity is the main task when designing the memory component. Normally, for addressing bottleneck problems, one channel's data needs many input/output (IO) pin connections that interface between the FPGA-chip and the off-chip memory component Static random-access memory (SRAM), such as for storing event information (energy and coarse time). The number of IO pins connected could be reduced if the data was written into the SRAM in more memory addresses. For example, the same 64-bit data could be written into 1 memory address in a situation with 64 pins or 4 memory addresses in a situation with 16 pins. However, this solution would significantly reduce the number of memory addresses. Fig. 2(c) shows the advantages of the counting mode in addressing the limitation of the hardware.

To address the previously mentioned issues and to maximize the parallel processing ability of the FPGA chip, an event counting function was added. Instead of storing each event with its energy value and coarse time, the event was counted before storing it in memory as the number of events in the predefined period. In this way, in the same 16-bit data, the counting mode could carry the information of a maximum of 65536 (2^{16}) events. Therefore, instead of several hundred megabytes of resources for each channel's data, the counting mode only requires several hundred kilobytes (Fig. 3(b)). Additionally, the number of FPGA IO pins connected with SRAM memory components could be handled easily.

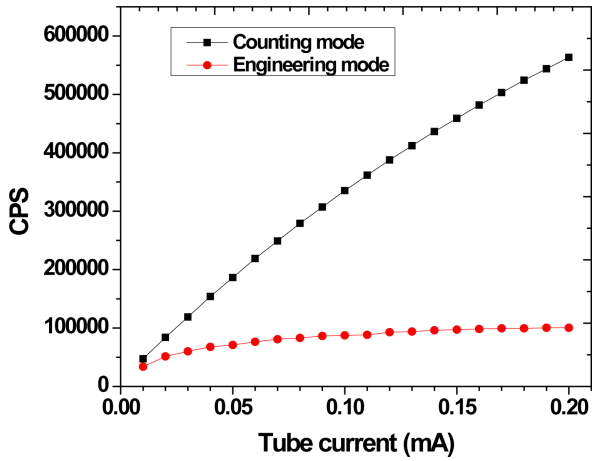

Fig. 4. (Color online) Comparison of CPS curves as a function of tube current. (black) Counting mode. (red) Engineering mode.

The count rates of the engineering and counting modes were examined for 1 minute with a tube current range of 0.01 to 0.2 mA in steps of 0.01 mA. Figure 4 clearly shows the significant difference between these two modes. Because of the time gap mentioned previously, the count rate in the engineering mode was considerably lower than in the counting mode and could not achieve the target required for DEXA scanning. This demonstrated the need for the counting mode.

4. Intrinsic Performance of Detector

4.1. Linearity and flood histogram

To examine the intrinsic performance of the DAQ system, a sinusoid pulse from a function generator was used, as a function of the pulse amplitude. As shown in Fig. 5(a), output linearity evaluated from voltage-peak channels was satisfactory for the whole input range. An estimated coefficient of determination (R^2) was 0.999. The voltage resolution was evaluated by FWHM obtained from the Gaussian fit, and no significant alteration in voltage resolution was observed. Fig. 5(b) shows the flood histogram and voltage-peak channels as a function of ADC-bit value.

4.2. Spectral response for gamma- and X-rays

Gamma-ray spectra from a radiation source (Am-241) were acquired for 30 min for the LYSO-GAPD detector module. A 1 mm diameter point source was set up 20 mm away from the top surface of the detector module. The energy spectra of the Am-241 are shown in Fig. 6(a). The observed photopeak of 59.5 keV was 620 mV and the

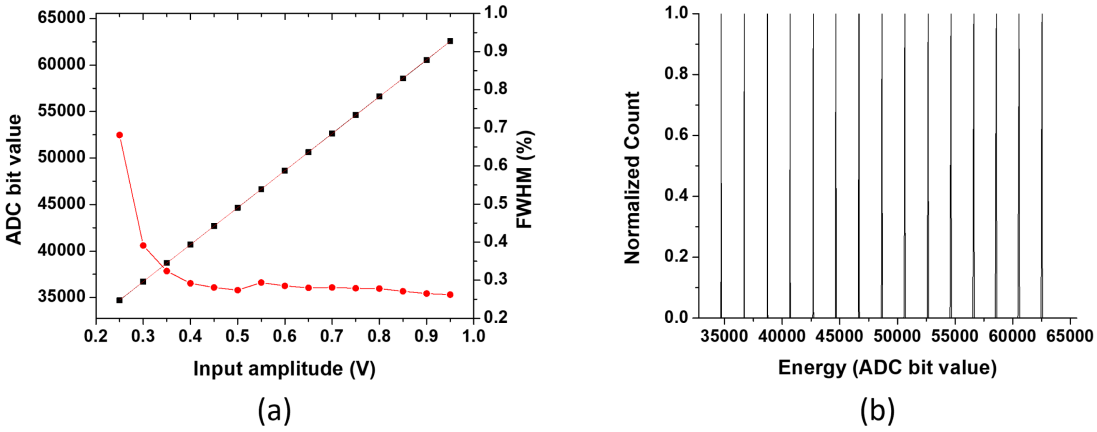

Fig. 5. (Color online) (a) Voltage-peak channel and Full Width at Half Maximum (FWHM) as a function of the amplitude of sinusoid input signal and (b) Flood histogram and voltage-peak channels as a function of ADC-bit value.

energy resolution evaluated by FWHM obtained from the Gaussian fit was ~28.2 %.

The dual-energy X-ray energy spectra of 8 input channels were acquired at a tube voltage of 80 kVp and a tube current of 0.01 mA. The dual-energy peaks were measured at 350 and 625 mV for low- and high-energy peaks, respectively (Fig. 6(b)). The spectra and CPS curves demonstrate the acceptable equality of the detector module. The separated low- and high-energy windows were set to 20 %, centered around their photopeak position. The CPS curves of the high- and low-energy bands as a function of the tube current of the 8 input it

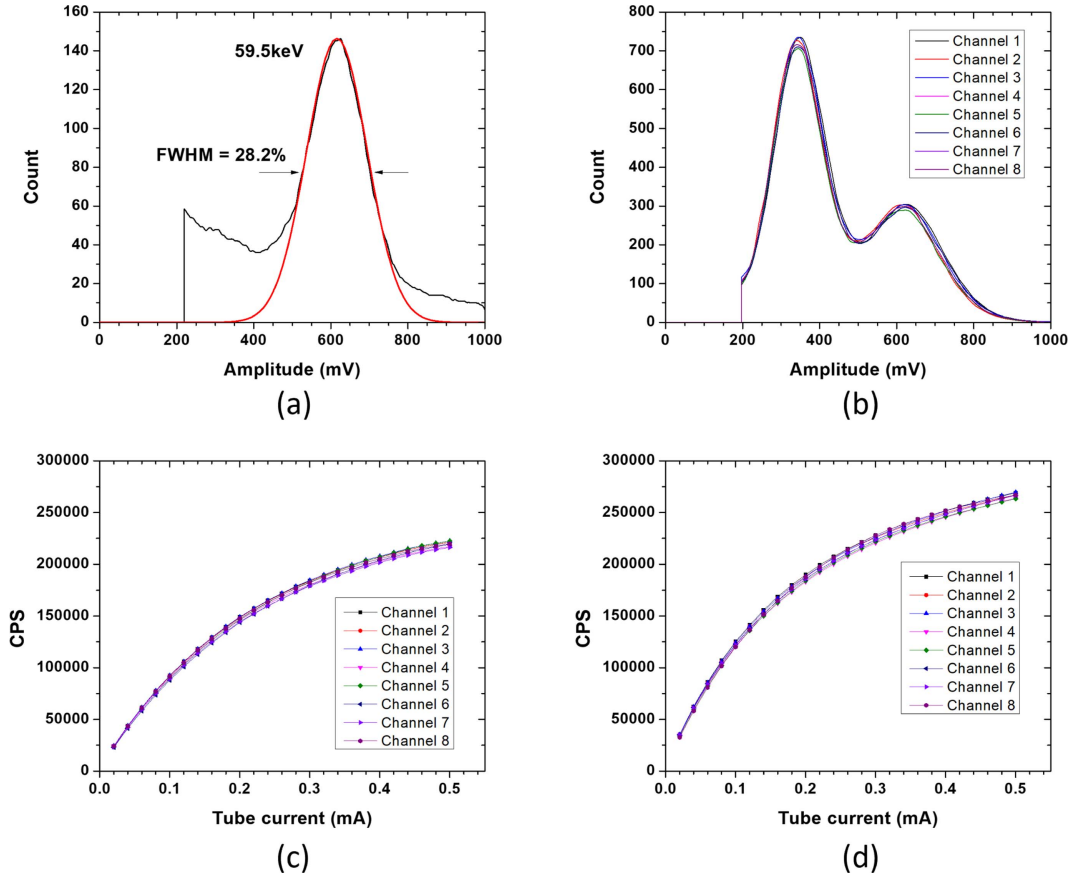

Fig. 6. (Color online) Acquired energy spectra of (a) Am-241 gamma-ray sources X-ray and (b) 8 channels dual-energy. CPS curves as a function of the tube current of 8 input channels. (c) Low-energy window. (d) High-energy window.

would be better described within page 5, by changing the figure size.

5. Image Performance

5.1. Scanning method

The data needed for examining and reconstructing images was the number of events in the low- and high-energy windows for each image pixel. After the energy of the events was calculated, it was compared with the predefined energy window to classify in which window (low or high) it belongs, as shown in Fig. 3. When the FPGA chip completed the acquiring time for a one-pixel row, the number of counted events for low- and high-energy were stored in the block ram, then those values are reset to 0 and it is ready for the next pixel row. When a whole scanning region was completed, the data of all pixels were transmitted to the PC for further processing.

5.2. Synchronizing method

The synchronizing timing of the DAQ and motion part was the most important key of the DEXA system, significantly affecting image performance. As shown in Fig. 7, at the starting point of each column, a 2.5 V pulse from the motion system operated as a synchronizing signal with a rise time of 1 μs, which was sufficient to appear as logic '1' for the FPGA input. Whenever the FPGA chip received this signal, it started running its timer based on a 125 MHz clock and simultaneously collected events in the low- and high-energy windows for each pixel image.

5.3. Acquired phantom images

A lumbar spine, encapsulated spine, and step wedge phantom (made from aluminum and acrylic for simulating bone and soft tissue) were used to characterize the image performance of the system. The lumbar spine, which simulated the human spine from T12 to L5, consisted of aluminum of different thicknesses in the range of 4.0 mm to 9.5 mm. The step wedge phantom consisted of 15 aluminum steps ranging from 1.2 to 6.8 mm with an increment of 0.4 mm in thickness. The encapsulated spine consisted of an aluminum block with different thicknesses ranging from 4 to 12 mm and 120 mm-thick solid acrylics as an encapsulated material. The X-ray source and detector module synchronously moved toward the column of the scanning field, and collected low- and high-energy events were acquired for 50 msec for each pixel row. The scanning time for an area of 70 × 160 pixels (pixel resolution of 1.05 mm × 1.05 mm) was 70 sec (excluding y-axis moving time). The dual-energy images were

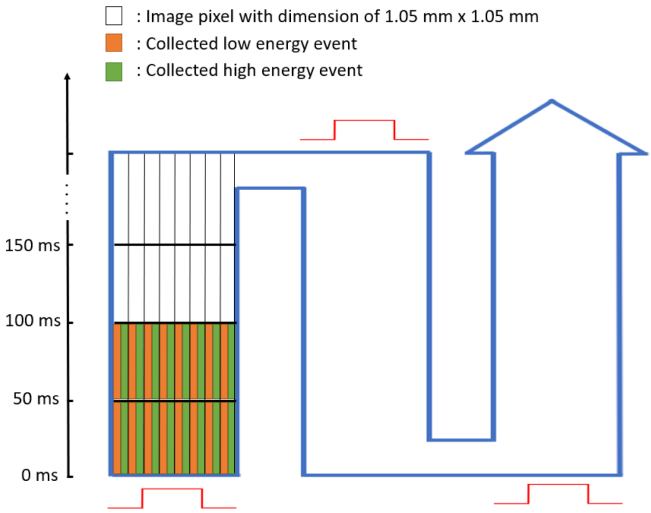

Fig. 7. Scanning route and timing synchronizing method.

reconstructed into density images by using a conventional dual-energy subtraction algorithm [17, 18]. The schematic diagram, the acquired image, the line profile, and the image intensity of each phantom are shown in Fig. 8.

Various phantom images were well imaged, and the shape, length, edge, and steps were well-characterized. The image intensity increased linearly from 0.62 to 1.58 for the lumbar spine, from 0.14 to 0.96 for the step wedge phantom, and from 1.7 to 2.3 for the encapsulated spine. The pixel resolution achieved 1.05 mm × 1.05 mm, which was limited by the geometric magnification factor of the DEXA scanner and the pixel dimension of the LYSO-GAPD detector used in this study.

6. Discussions

The X-ray exposure condition with a tube voltage of 80 kVp and a tube current of 0.1 mA was quite low in this study, compared with current commercial DEXA systems. Although made in the form of an array with more scattering, the ~28.2 % energy resolution at a peak of 59.5 keV (Am-241) was superior to the 34 % of the NI-DAQ PIX-1033 that was studied in the previous research using a similar detector configuration [20]. The LYSO crystal, with its good characteristics of fast-decay time (~40 ns) could work in high count rate experiments. Moreover, current FPGA designs could run effectively at normal count rates when the pile-up effect is insignificant. To address this effect, which appears when running at relatively high-count rates scanning [17, 18], some research into analog signal processing is needed to remove or shorten the falling-edge period. In such cases, the FPGA logic for calculating energy (which is presented

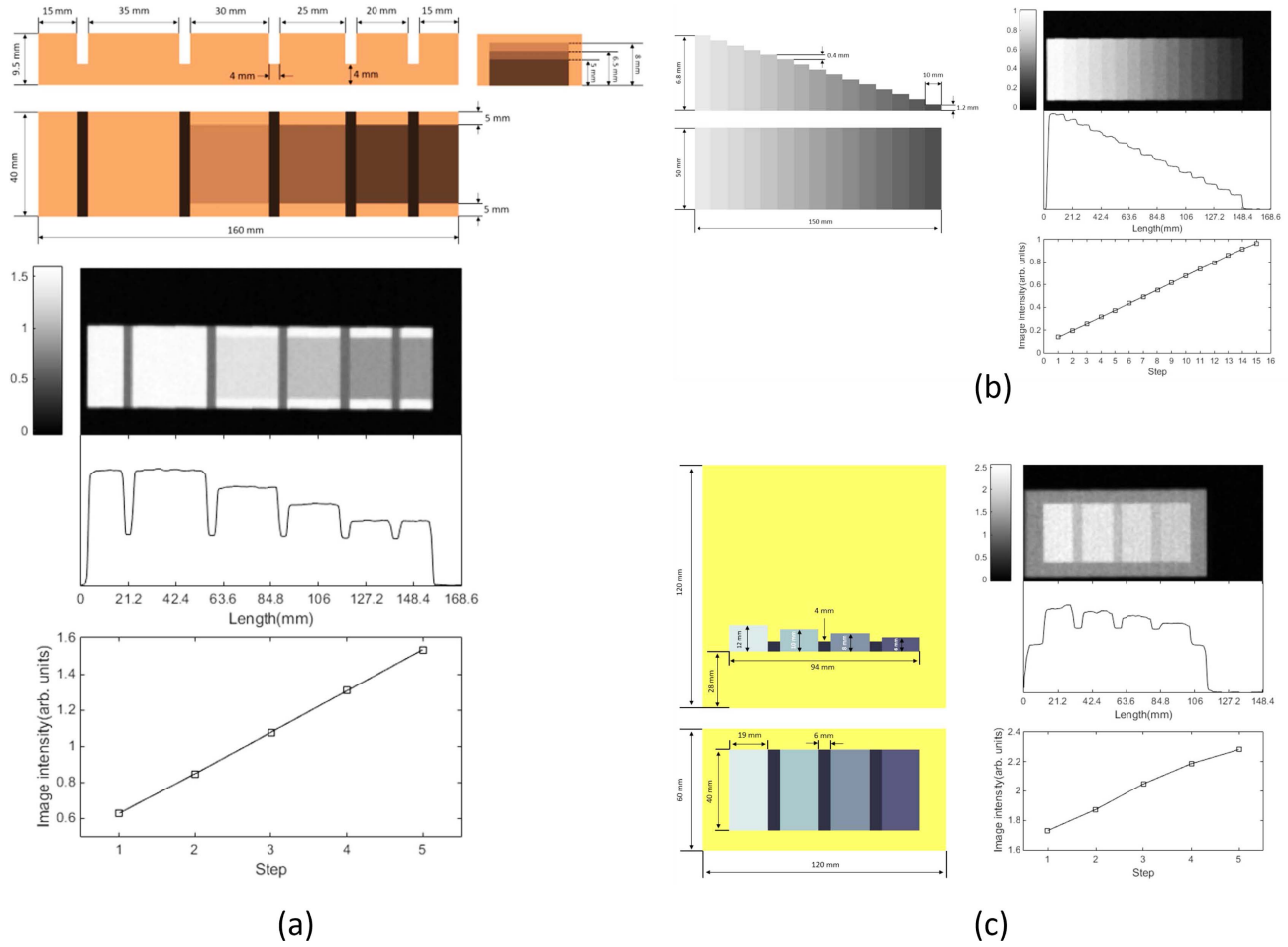

Fig. 8. Schematic diagram, acquired image, line profile, and image intensity of (a) Lumbar spine Phantom, (b) Step wedge phantom, and (c) Encapsulated spine phantom.

Table 1. FPGA chip device utilization summary.

Slice logic utilization	Used	Available	Utilization
Number of Slice Registers	4,841	93,120	5 %
Number of Slice LUTS	3,907	46,560	8 %
Number of bonded IOBs	204	360	56 %
Number of RAMB36E1 (Block Ram)	128	156	82 %

in this project) would be adjusted (e.g., remove the 450 ns pause time) to facilitate high count rate scanning [18, 19]. Furthermore, studies could be conducted on applications with human targets, with the radiation dose and the scanning time appropriately reduced.

Not all FPGA boards are designed to work effectively with multiple channels. Ideally, a single SRAM for each channel is employed to prevent bottlenecks problem. Assuming that the target is 64 channels, each SRAM requires approximately 40 IO pins (address and data) to interface with the FPGA chip. This means the FPGA chip would require nearly 2500 IO pins just for connecting to the SRAM components, which is impossible with current FPGA technology. If multi-FPGA chips with the same function could be used to share the workload of one chip, the board would be very complex and not cost-effective. Given the target of designing a cost-effective DAQ for DEXA, the counting mode presented in this paper must be applied to guarantee that all events are processed in the complete scan without off-chip SRAM components. A typical solution to address the limitation of data transmission rates between the board and PC is PCI express. However, this is not the ultimate solution and increases the complexity of the board. As shown in Table 1, the on-chip memory resources are 82 % for a maximum of 131,072 image pixels (1310 cm^2 for a pixel dimension of 1 mm). If a larger resource is required for scanning, one additional SRAM could be used. This solution is possible because unlike the bottleneck problem in engineering

mode, where events (data) randomly happen, the stored data of all channels (the number of events for low- and high-energy for each pixel) in counting mode could be written into RAM in a continuous address. It should be noted that the FPGA chip used in this project was the Xilinx Virtex-6 FPGA (XC6VLX75T-2FFG784C), which is the weakest in the Virtex-6 device family. The number of IO pins used in this design is 204/360, which includes 16 I/O pins for the 8 ADC channels and the remainder are for controlling and communicating functions. Moreover, this design uses a small part of the FPGA's parallel calculation ability, which is demonstrated by the number of slice registers and the number of slices LUTS (Table 1). This demonstrates that a DAQ system for a 64-channel fan-beam DEXA could be built based on this FPGA chip. This counting mode design will prove its value as the number of signal channels increases. The details presented in this paper prove the feasibility of building a cost-effective DAQ system that could process multichannel in a fan-beam DEXA system.

7. Conclusions

In this study, we built and evaluated the FPGA-based DAQ system to process 8 input signals simultaneously from the LYSO-GAPD detector module to achieve ~1 mm image pixel resolution in the fan-beam DEXA instrumentations developed by our group. The possibilities and cost-effectiveness of designing a DAQ with a simple ADC and FPGA board for a multichannel scanner were demonstrated. Accordingly, it would be a possible component of DEXA instrumentation running in both research institutions and hospitals.

Acknowledgments

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