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Multilevel Inverters Power Topologies and Voltage Quality: A Literature Review

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Due to their performances and inherent benefits, especially in medium-voltage and high-power applications, multilevel inverters have received an increasing attention in real world industrial applications. The present paper deals with a review of the main multilevel inverter topologies as well their most common derived and hybrid structures quoted in previous research works. It also encompasses an investigation on voltage harmonic elimination and THD estimation. For that reason, the paper summarizes the most relevant modulation techniques used so far to enhance the output voltage quality. Theoretical formulas evoked in the literature, for calculating the output voltage THD upper and lower bounds are reported and verified by adequate simulations.

Keywords : multilevel inverter topologies, modulation, control algorithms, voltage quality bounds, Total Harmonic Distortion (THD)

1. Introduction

Multilevel inverters are DC-AC static power converters exhibiting at their output terminals more than two-level voltage waveforms. Nowadays they find increasing attention especially for medium-voltage and high-power applications [1, 2]. In the mid 1970's, Baker and Bannister have proposed the first multilevel inverter [3]. It consists of series connected single phase H-bridges. Later, Nabae *et al*. developed another multilevel inverter called 3L-NPC (Neutral Point Clamped diodes) [4]. In such topology, several diodes ensure levels construction of output voltage by linking capacitive sources to switches. Following the NPC, a Flying Capacitors topology (FLC) was proposed by putting clamping capacitors instead of diodes [5]. As a consequence, cascaded H-bridge, NPC and FLC are the basic and most used multilevel inverters. After that, multitude of derived and hybrid multilevel topologies were introduced [6-16]. However, they still on the shadow of the major multilevel configurations previously stated. The most industrialized multilevel topologies are the three-level NPC (3L-NPC), the cascaded H-bridge (ML-CHB), and the four-level flying capacitors (4L-FLC) [17].

Typically, multilevel topologies have been used to overcome the limitations of conventional two-level inverters. Particularly, the voltage stress on switching devices is decreased by putting in series power switches. The total harmonic distortion is reduced by adding steps or levels in the output voltage waveform fitted with the sinusoidal reference. In practice, this is achieved by multiplying the number of DC sources and also by considering their terminals as positions to be switched [18].

Multilevel inverters features have several other promising advantages over two level topologies such as: i) the possibility to overcome the problem related to the maximum voltage drop of the main power semiconductors. ii) Transformer-less inverter architecture desirable in renewable energy applications [19]. iii) Reduction of the common mode voltage which causes inherent damages of the bearings. iv) High resolution of the output waveforms [20, 21]. Therefore, the voltage adjustment is smooth which reduces the stress on the load, otherwise the voltage in conventional inverter varies between two values. The rating of passive filters, sometimes necessary to limit these stresses, can be also reduced. Consequently, the system wins more dynamic and allows faster regulation. v) Minimized electromagnetic interference issues [22].

Multilevel inverters applications cover mainly the variable speed area as motors drives [23-26], pumps [27], conveyors [27, 28] and electric traction [29-31]. Multilevel inverters are also used for electrical power conditioning as voltage rectifier, static compensator (STATCOM), Back to Back inverter connected to the network [32-35]. Recently, they are associated with renewable energy systems in photovoltaic

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applications and wind generation [22, 36-39]. Thanks to the development of semiconductors dedicated to high power, particularly IGBTs at 3.3 kV, 4.5 kV and 6.5 kV, the power ranges associated to multilevel inverters were significantly extended to medium and high voltages (2-13 kV).

Regarding control algorithms, the frequently used techniques are Selective Harmonic Elimination (SHE) and Pulse width modulation (PWM) [40]. Advanced methods developed thereafter are improvements of those above. PWM-based techniques are most relevant in industrial field including multi carriers and space vector modulation. With those techniques, we can reduce switching losses and achieve a low total harmonic distortion, so better voltage quality.

Elsewhere, the present review paper is enhanced by introducing Ruderman works [41-44]. These latter allow the estimation of the total harmonic distortion based on a time study instead of frequency domain. This can remedy THD's estimation errors especially for high frequency switching. Contrary to what is common, Ruderman demonstrated that, in case of three-phase balanced load with isolated neutral, THDs of both line and phase voltages are the same. He also established intuitive simple hyperbolic formulas which may be used as a reference to calculate reliable multilevel converter voltage THDs. To our knowledge, this interesting approach is the first time addressed in a review paper.

The present paper is organized in a way so that it could serve as reference for inverter specialists as well as for newly introduced in the field. Taking apart the introduction and the conclusion, section 2 gives a general overview of the main multilevel topologies mentioned in the literature (H-Bridge, NPC, FC) with their operating principle and associated mathematical models. In section 3, some of common derived configurations are reported. Examples of hybrid structures are detailed in section 4. Finally, section 5 is devoted to the output voltage quality analysis.

2. Multilevel Inverters Main Topologies

2.1. Cascaded full bridge inverter

Cascaded full bridge multilevel inverters are also called series connected H-bridge or cascaded H-bridge. It consists in connecting in series single-phase H-bridges. Each single-phase inverter is a full partial cell formed by four bidirectional switches (MOSFET, IGBT or GTO + free-wheel diode connected in antiparallel) and a DC voltage source E. The output voltage generated by an H-bridge has three levels (–E, 0, E). The DC power supplies must be specific

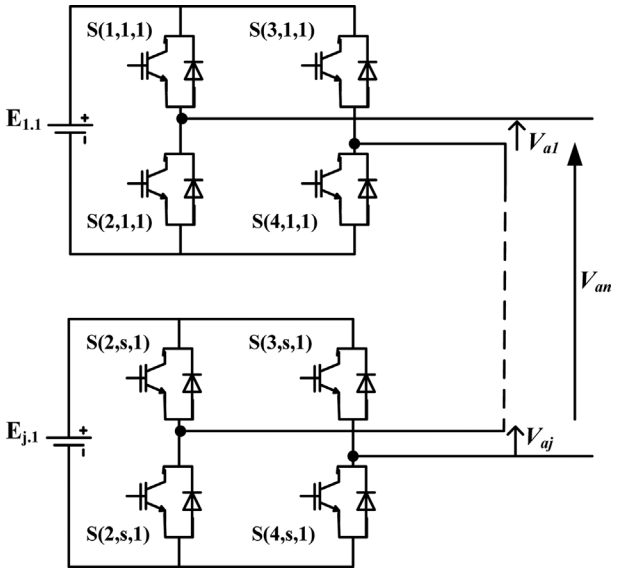

Fig. 1. Topology of an H-bridge arm composed by *S* cells connected in series.

or dedicated to each single-phase bridge and electrically isolated from each other [45]. This allows overcoming problems related to charge balancing of the DC link capacitors as in NPC topologies and prevents unwanted short circuits across the capacitors.

The generalized topology of an *m* level H-Bridge arm is shown in Fig. 1. The nomenclature of this structure is as follows:

- The switch $S(i, j, k)$ is the i^{th} switch of the j^{th} cell belonging to the k^{th} phase.
- The DC source $E_{j,k}$ is the voltage source supplying the j^{th} cell of the k^{th} phase.
- (V_{aj}, V_{bj}, V_{cj}) are the output voltages of the j^{th} cell respectively of the first, second and third phase.
- (V_{an}, V_{bn}, V_{cn}) are respectively the phase voltages of the first, second and third arm.
- *S* represents the cell number.

The stepped voltage waveform is composed by m levels which depends on the DC sources number such that $m = 2S+1$. Thus, whatever the type of cascaded multilevel inverter is, the output voltage levels number is always odd (3, 5, 7, 11...). The different H cells are connected in series so that the resulting voltage of an arm is equal to the sum of all voltages generated by each cell:

$$V_{an} = \sum_{i=1}^{s} V_{ai} \tag{1}$$

For $S = 2$, the three phase and line output voltages can be expressed as follows:

$$\begin{cases} V_{an} = E * \sum_{j=1}^{s} \left[S(1,j,1) + S(4,j,1) - 1 \right] \\ V_{bn} = E * \sum_{j=1}^{s} \left[S(1,j,2) + S(4,j,2) - 1 \right] \\ V_{cn} = E * \sum_{j=1}^{s} \left[S(1,j,3) + S(4,j,3) - 1 \right] \end{cases} \quad (2)$$

$$\begin{cases} U_{ab} = E * \sum_{j=1}^{s} \left[(S(1,j,1) + S(4,j,1)) - (S(1,j,2) + S(4,j,2)) \right] \\ U_{bc} = E * \sum_{j=1}^{s} \left[(S(1,j,2) + S(4,j,2)) - (S(1,j,3) + S(4,j,3)) \right] \\ U_{ca} = E * \sum_{j=1}^{s} \left[(S(1,j,3) + S(4,j,3)) - (S(1,j,1) + S(4,j,1)) \right] \end{cases} \quad (3)$$

2.2. Neutral point clamped diode

The first structure, namely the three-level NPC, was first introduced by Nabae in the 80's [4]. The NPC inverter is built by using several continuous buses having equal capacities fed by only one DC power supply as depicted in Fig. 2. The presence of clamping diodes links each pair of switches to a bus for the purpose to build voltage levels within their switching order. These diodes also ensure current reversibility.

For an *m*-level NPC inverter, the number of capacitors, power switches and diodes needed for each leg are defined as:

- Number of capacitors: C = m–1
- Number of power switches : K = 2(m–1)
- Number of clamping diodes: D = 2(m–2).

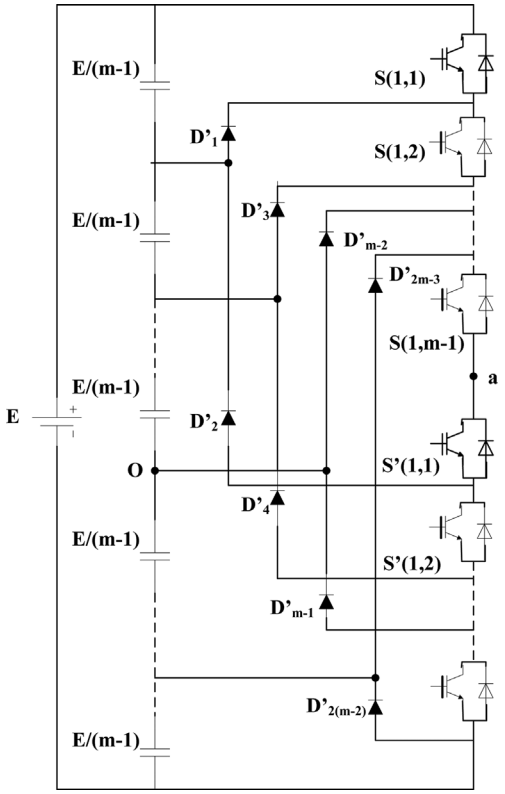

Fig. 2. Topology of an *m*-level NPC leg.

It should be noted that each couple of switching devices ($S(1, j)$, $S'(1, j)$) commutates in a complementary way. The output voltage V_{ao} generated by the first leg of the converter can be expressed by:

$$\begin{aligned} V_{ao} &= \pm K' \frac{E}{m-1} \\ K &\in \left[0, \frac{m-1}{2} \right] \end{aligned} \quad (4)$$

S_{ah} is the switching sequence of the first leg a. The switches $S(1, j)$ and $S'(1, j)$ commutate in the sequence given by equation (5). As example, for h = 1 (first switching sequence), $S_{a1} = S(1,1) + S(1,2) + S(1,3) + S(1,4)$, which gives $V_{ao} = E/2$.

$$\begin{aligned} S_{ah} &= \sum_{j=K}^{m-1} S(1,j) - \sum_{j=1}^{K-1} S'(1,j) \\ h &\in [0, m] \end{aligned} \quad (5)$$

Regarding the possible switching states, the corresponding output voltage, referred to the middle point o for each leg, can thereafter be expressed as:

$$\begin{cases} V_{ao} = (2 * \sum_{j=1}^{m-1} S(1,j) - (m-1)) \frac{E}{2(m-1)} \\ V_{bo} = (2 * \sum_{j=1}^{m-1} S(2,j) - (m-1)) \frac{E}{2(m-1)} \\ V_{co} = (2 * \sum_{j=1}^{m-1} S(3,j) - (m-1)) \frac{E}{2(m-1)} \end{cases} \quad (6)$$

Expressions of phase to neutral and line to line output voltages are given by (7) and (8) respectively:

$$\begin{cases} V_{an} = \frac{E}{3(m-1)} \left[2 * \sum_{j=1}^{m-1} S(1,j) - \sum_{j=1}^{m-1} S(2,j) - \sum_{j=1}^{m-1} S(3,j) \right] \\ V_{bn} = \frac{E}{3(m-1)} \left[-\sum_{j=1}^{m-1} S(1,j) + 2 * \sum_{j=1}^{m-1} S(2,j) - \sum_{j=1}^{m-1} S(3,j) \right] \\ V_{cn} = \frac{E}{3(m-1)} \left[-\sum_{j=1}^{m-1} S(1,j) - \sum_{j=1}^{m-1} S(2,j) + 2 * \sum_{j=1}^{m-1} S(3,j) \right] \end{cases} \quad (7)$$

$$\begin{cases} U_{ab} = (\sum_{j=1}^{m-1} S(1,j) - \sum_{j=1}^{m-1} S(2,j)) \frac{E}{(m-1)} \\ U_{bc} = (\sum_{j=1}^{m-1} S(2,j) - \sum_{j=1}^{m-1} S(3,j)) \frac{E}{(m-1)} \\ U_{ca} = (\sum_{j=1}^{m-1} S(3,j) - \sum_{j=1}^{m-1} S(1,j)) \frac{E}{(m-1)} \end{cases} \quad (8)$$

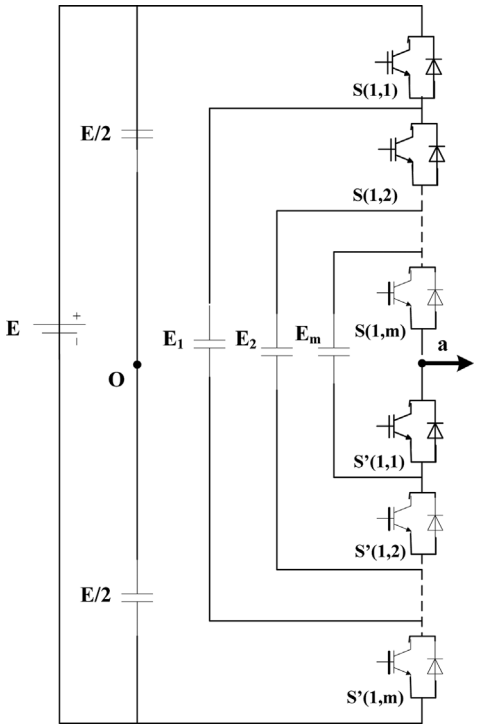

Fig. 3. Topology of an *m*-level Flying Capacitors leg.

2.3. Flying capacitors

This topology was proposed by T. Meynard and H. Foch in 1992 [5]. It is also known as nest cell converter because it is divided into several cells nested inside each other. Clamping capacitors is also another name that can be found in the literature [46]. A cell consists of a capacitor and a complementary pair of switches, as depicted in Fig. 3. This inverter alleviates the clamping diodes issues by substituting them with capacitors. These latter are connected in series with the DC power supply because the absence of diodes makes impossible to connect directly the load to the desired DC voltage. The 'clamping capacitors' help to keep constant the voltage drop between busses to which they are connected [47]. For an *m*-level flying capacitors inverter the number of capacitors, power switches, and commutation cells needed for each leg are defined as:

- Number of capacitors: C = m–1
- Number of power switches : $K = 2(m-1)$
- Number of commutation cells: $D = m$.

Converter typical voltages are:

$$\begin{cases} V_{ao} = -\dfrac{E}{2} + \sum_{j=1}^{m-1} S(1,j)\dfrac{E}{(m-1)} \\ V_{bo} = -\dfrac{E}{2} + \sum_{j=1}^{m-1} S(2,j)\dfrac{E}{(m-1)} \\ V_{co} = -\dfrac{E}{2} + \sum_{j=1}^{m-1} S(3,j)\dfrac{E}{(m-1)} \end{cases} \quad (9)$$

$$\begin{cases} U_{ab} = (\sum_{j=1}^{m-1} S(1,j) - \sum_{j=1}^{m-1} S(2,j))\dfrac{E}{(m-1)} \\ U_{bc} = (\sum_{j=1}^{m-1} S(2,j) - \sum_{j=1}^{m-1} S(3,j))\dfrac{E}{(m-1)} \\ U_{ca} = (\sum_{j=1}^{m-1} S(3,j) - \sum_{j=1}^{m-1} S(1,j))\dfrac{E}{(m-1)} \end{cases} \quad (10)$$

3. Multilevel Inverters Derived Structure

3.1. H-Bridge derived structures

To reduce the number of bulky DC sources, new classes of cascaded H-bridge were proposed. The asymmetric full bridge inverters were an alternative. They have the same configuration as the cascaded symmetrical inverters except that continuous sources values are not equals but multiples of each other's [6]. Generally, the DC sources are multiples of two (2E, 4E...), Fig. 4. Thus, the number of output voltage levels increases up to $2^{(n+1)}$–1.

Furthermore, according to [20], an H-bridge inverter can easily operate with only one isolated DC power source; the other sources may be replaced by capacitors. Consequently, this topology requires a specific control strategy to regulate the voltage across the capacitors [8].

Modular Multilevel Converter (MMC) is also an innovative structure in the HVDC family which idea is inspired from cascaded H-bridge inverter. This topology provides output waves with high number of levels that can be extendable to any desired one with adjustable AC voltage magnitude [9, 10]. Siemens integrated the first MMC in electric power grid application as HVDC PLUS. Each arm is constructed out of sub modules connected in series. A sub module can be a half or a full bridge supplied by a capacitor.

The upper or lower half of a phase is called multivalve

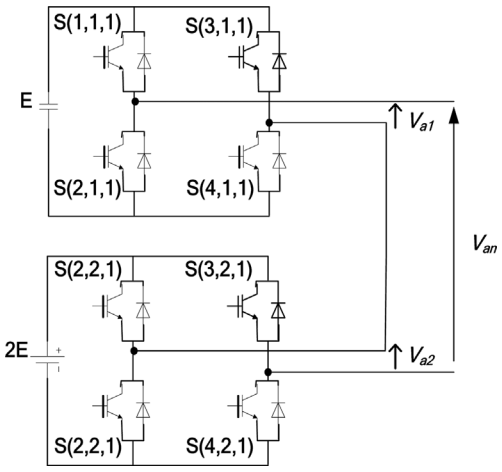

Fig. 4. Topology of an asymmetric H-Bridge arm.

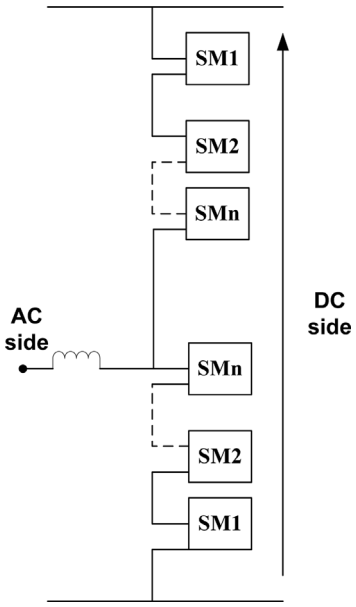

Fig. 5. Architecture of a MMC multilevel converter.

as shown in Fig. 5. The converter arm acts like a flexible controllable voltage source since a sub module can be controlled selectively or individually. Among the MMC features, we mention a reduced voltage drop, the use of non-Phase Shifted transformers with low insulation, high reliability due to the modular structure.

3.2. NPC derived structures

Various modified NPC topologies have also been proposed in the literature in recent years. For example, new reduced topologies have been developed in [11] so as to achieve less cumbersome converters in terms of number of components and ride through the unequal losses distribution in the switches. In [12], the authors added devices using IGBTs in parallel with the clamping diodes allowing this structure to have multiple control modes, Fig. 6a. For instance, it is possible to choose the modulation type for balancing losses. An active NPC topology (ANPC) was proposed in [13]. By adopting a modified PWM strategy, this topology is able to double the apparent switching frequency and enhances the loss distribution balance in semi-conductors. In addition, it enables the inverter to operate under conditions of high and low switching frequencies.

A Stacked ANPC inverter was proposed in [11] by adding in each arm, between the load and the neutral point, a branch made of two switches in series as shown in Fig. 6b. Therefore, many redundancies creating the intermediate level can be achieved which allows increasing the apparent switching frequency when compared to the ANPC topology. This topology offers the advantage of

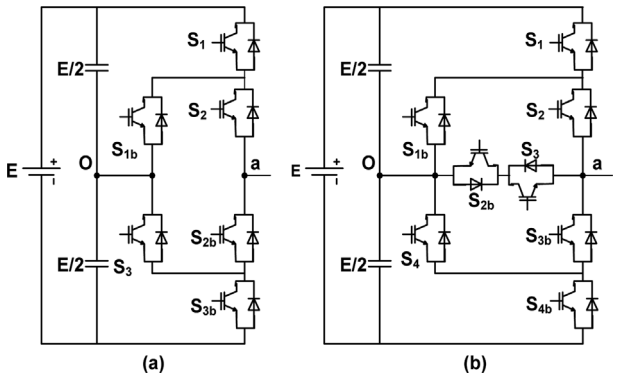

Fig. 6. (a) Active NPC topology. (b) Stacked ANPC topology.

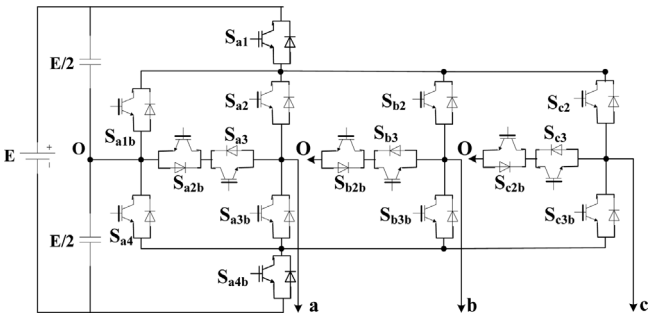

Fig. 7. SASNPC topology.

using less switching devices with respect to the two previous structures. Although the possibility of doubling the apparent switching frequency is no longer possible, redundancies can still be used to allocate losses in the different components or even to limit the switching losses by trying to commutate the fewest devices [14]. However, all the aforementioned NPC variants remain bulky and complex in terms of control. A shared NPC topology SASNPC was proposed in [14]. Its main feature remains, in the fact, that the three arms of the inverter share both upper and lower switches as depicted in Fig. 7. As at any time three transistors should be turned on, therefore eight possible combinations of the switch states can be synthesized. Among these combinations, two zero redundant states (V_0) and six active states (V_1, V_1-V_2, V_2, 0, -V_2, V_2-V_1, and -V_1) can be applied across the load. Table 1 below gives the number of active and passive components

Table 1. Active and passive components per phase for seven-level FC and PU Cells inverters.

	FC	PU Cells
Switches	12	6
Capacitors	6	2
Clamping diodes	0	0

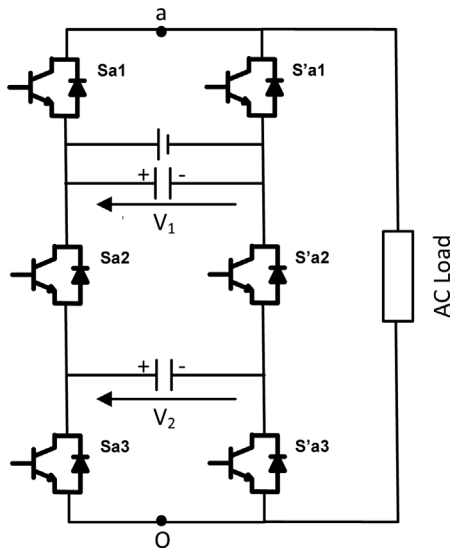

Fig. 8. Seven-level Packed U-cells leg.

(per phase) required for basic FC, topology and PU cells. As can be seen, the PU cells topology has several advantages over the other ones. Compared to the seven-level flying capacitors basic topology, the number of capacitors is reduced from 6 to 2. Moreover isolated DC sources are not compulsory.

3.3. FC derived

A general power circuit of a seven level packed U cells converter (Only one phase) is depicted in Fig. 8. Only two capacitors are required for each leg. The first one is used in parallel with the DC power source (V_1). Whereas the second allows, with the use of a control circuit, the generation of a regulated voltage level (V_2) which is necessary to produce the exact voltage levels across the load [15]. As can be seen, only six power switches are required for each leg. Each couple of switches $S_{ax(x=1,2,3)}$ and S'_{ax} are turned on in a complementary manner.

4. Multilevel Inverters Hybrid Topologies

Generally, the cascaded H-bridge multilevel inverter is the basic topology subject to hybridization by simply exchanging a bridge by another of a different type. For the purpose of mastering the voltage capacitors unbalancing problems which appear with the 5L-NPC as well as with DC sources isolation of the H-Bridge, a compromise was established when developing a mixed topology formed by 3L-NPC cells connected in cascade [48]. The resulting topology called cascaded 5L-NPC inverter produces thus a five levels output voltage with a more compact structure and controlled DC voltage sources. In [49], the authors

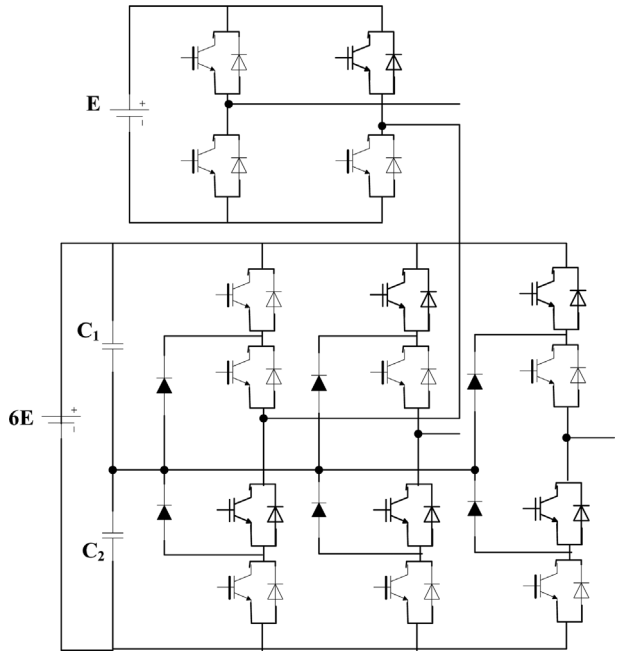

Fig. 9. Hybrid multilevel inverter leg proposed by Manjrekar *et al.*

improved the output waveform quality which has been increased to 9 by using the same number of cells.

Manjrekar *et al.* proposed in [50] to combine three single-phase cells and a three-phase inverter NPC as depicted in Fig. 9. This will reduce congestion because the DC sources decrease from six to four, generating in addition a voltage of nine levels.

Another similar approach was presented by Suh *et al.* [51]. The second H-bridge cell is substituted by a conventional three-phase inverter. Like the previous topology, this approach decreases the number of components mainly the DC power sources compared to the inverter mentioned above. Contrary to all structures in cascades, the output voltage has an even number of levels.

A symmetrical hybrid multilevel converter with reduced number of insulated DC sources is proposed in [52]. This topology is a combination between the NPC and H-bridge inverter, Fig. 10. A full bridge is integrated to an NPC main structure. The bridge's switches operate at low frequency switching. This structure is advantageous over the conventional cascaded multilevel inverter since it needs a reduced number of isolated DC sources. Moreover, the switches number still the same. The three phase configuration of this inverter has two common points, one to connect the inverter legs and the other one is for load coupling. The line output voltage levels number is 2n+1 where n is the DC source number. It is obvious that the asymmetry in the DC voltage sources requires special care. The power switches must withstand different rates

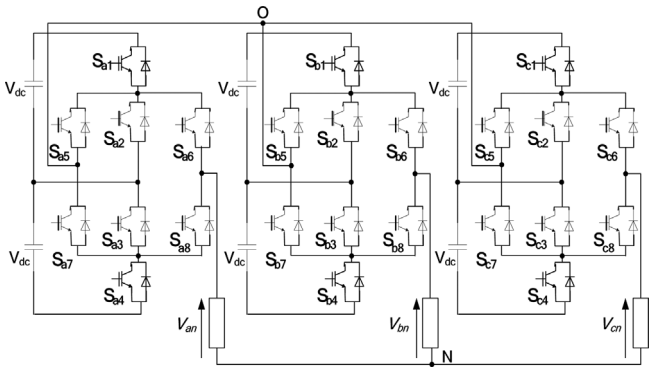

Fig. 10. Symmetrical hybrid multilevel inverter with reduced DC supplies.

of voltage stress. In this case, the use of devices belonging to distinct families is needed. The IGCTs (Integrated Gate-Commutated Thyristors) and HV-IGBTs (Insulate Gate Bipolar Transistors) are more appropriate for cells operating at high voltages [53], thanks to their large voltage blocking capacities (over 4.9 kV), their high efficiencies and their reduced losses [53]. For instance, LV-IGBTs have good performances when operating at low frequencies [54]. Therefore, the concept of hybrid no longer concerns the concept of architecture but also includes the integration of semiconductors of different types in the same topology.

5. Voltage Quality Analysis

5.1. Voltage harmonics elimination

Modulation techniques are applied with the purpose of controlling the inverter's output voltage and frequency as well as to improve the quality of output waveforms. They are divided into two main categories [54]:

- Operation at fundamental switching frequency: Selective Harmonic Elimination (SHE).
- Operation at high switching frequency: Pulse Width Modulation (PWM) and Space Vector Modulation (SVM).

5.1.1. Selective harmonics elimination

This method, as its name suggests, is based on the elimination of chosen harmonics generally dominant ones at low frequencies. The aim of SHE is therefore to reduce the total harmonic distortion THD of the output waveforms [55]. It consists in decomposing the target output waveform into Fourier series. A system of transcendental equations depending on switching angles (θ_1..... θ_n) is thereafter established. The resolution of this system is done by calculating the opportune angles (θ_1..... θ_n) using the Newton-Raphson method. The number of calculated angles is equal to the one of isolated sources in the case of the SHE at the fundamental switching frequency and it is different in the case of the SHE at high switching frequency [48]. It should be underlined that this method could also be used at high switching frequencies (SHE-PWM). However, resolution of transcendental equations becomes more complex. The Newton-Raphson method is not efficient because it requires good prediction of initial states. Recent algorithms were developed allowing more accurate solutions by mean of Walsh functions [56] or neural networks [57].

5.1.2. Pulse width modulation

In this case, Modulation techniques are based on sinusoidal PWM with multiple carriers. This method consists in comparing a sinusoidal signal called also modulating waveform with multiple triangular signals or carrier waves. The switches of each leg need (m-1) triangular signals having the same frequency f_p and the same amplitude A_p. The reference sine waves are phase shifted by $2\pi/3$. Their amplitude and frequency are denoted A_m and f_m. The sinusoidal PWM technique is characterized by two ratios, the frequency modulation index $m_c = f_p/f_m$ and the modulation ratio $m_a = A_m/((m\text{-}1)A_p)$. Various PWM modulation methods have been reported in the literature including Phase Opposition Disposition (PO-PWM), Alternate Phase Opposition Disposition (APOD-PWM), and Phase Disposition (PD-PWM) [58, 59]. All the aforementioned methods are based on PWM with multiple carriers but they differ in the triangular signals disposition such as:

- POD-PWM: the inner carriers around zero are 180° out of phase. Moreover, each couple of triangular signals above and below zero is in phase.
- APOD-PWM: every two subsequent carriers are phase shifted by 180°.
- PD-PWM: all the carriers are in phase.

5.1.3. Space vector modulation

The Space Vector Modulation (SVM) technique uses a space vector that represents the three reference output voltage waveforms. Hence, a space vector modulation algorithm should determine at each sampling time the appropriate switching states that best approximate the reference vector. In general this vector is synthesized by using a combination of the nearest two active voltage vectors and a zero vector [60-64].

The SVM is convenient for digital implementation on digital signal processors and allows high quality output waveforms with improved harmonic content. The implementation of a SVM involves three steps.

- Identification of the triangle in which the tip point of the reference vector is lying.

- Calculation of duty cycles for each triangle.
- Identification of switching states according to a desired switching sequence. In general, the approaches proposed in the literature differ mainly in the way of locating the reference vector. Among the few research works proposed in literature, we find in [61] an interesting approach that allows the direct identification of the adequate triangle wherein the tip point of the reference voltage vector falls. In [62] the authors start from the fact that the space-vector diagram of a three-level inverter is composed of six small hexagons that are the space-vector diagrams of two-level inverters. These small-hexagons are identified by dividing the space vector diagram into six sectors as shown in Fig. 9.

At any sampling time the reference voltage vector is located within these six small-hexagons, after that a new reference voltage vector must be defined. In this way, the three-level space-vector is simplified to a two-level space-vector. It should be noted that when the number of levels increases, the use of this algorithm becomes tedious.

Another approach applied to three-level inverters has been proposed in [63] where the space vector diagram of a three-level inverter was transformed from (α, β) frame to a hexagonal coordinate system (h, g). It follows that all switching vectors have integer coordinates. The reference voltage vector is thereafter located within an equal-sided parallelogram which makes easy the identification of the three nearest vectors. An alternative space vector approach was proposed in [60], where an m-level reference voltage vector has been constructed from the lower level reference vector.

In [60], the authors considered that the space vector diagram of an m-Level inverter has a fractal structure, where the basic structure is a triangle. Each sector was considered as a large triangle. By using fractal theory, each triangle was divided into four small triangles. The authors proposed thus a triangularization algorithm for identifying the appropriate triangle that encloses the tip point of the reference voltage vector. It should be noted that the number of iterations of triangularization algorithm becomes much higher as the number of levels increases.

5.2. Voltage quality bounds

According to the available literature, the only works defining and quantifying the THD bounds of multilevel inverters output voltages are those of Ruderman in [41-44]. The author argues that many recent multilevel inverter papers end up with voltage THD evaluation results that are typically based on voltage frequency spectra numerical calculations/measurements (FFT). A potential issue is a limited number of accounted harmonics. For example,

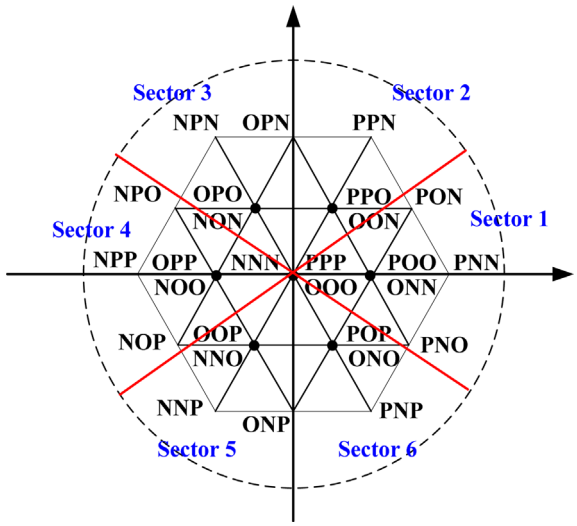

Fig. 11. (Color online) Small hexagons constituting the space vector diagram.

accounting for 49 harmonics (as recommended by IEEE Standard 519) may deliver essentially underestimated voltage THD. Numerically calculated line (line-to-line) and phase (line-to-neutral) voltage THD for a three-phase balanced load with isolated neutral may become different. However, though line and phase voltage spectra are different (triplen harmonics do not appear in the line voltages), line and phase voltage THD in this case are essentially the same that is almost evident from a time domain consideration [42]. Given numerically calculated or measured voltage THD, it may be difficult to judge about voltage quality whether it is good enough or bad? Does the voltage THD be subjected to the calculation or measurement errors? Therefore, it is instructive to elaborate theoretical bounds for optimal nearest switching voltage quality.

As mentioned previously, voltage quality for single and three-phase multilevel inverters with high switching frequencies was considered in [41-44]. The assumption of infinitely large switching frequency has led to an upper bound of voltage quality for synchronous nearest switching. In contrast, the lower voltage quality bound was achieved for a minimal amount of synchronous switching between any two adjacent voltage levels. The author approximated smooth THD upper and lower bounds by (11) and (12).

$$THD_{up}(L,M)=\frac{57.7}{(L-1)M},\ \%\tag{11}$$

$$THD_{low}(L,M)=\frac{47}{(L-1)M},\ \%\tag{12}$$

Fig. 12 exhibits an example of upper and lower bounds hyperbolic curves as function of modulation index for 3

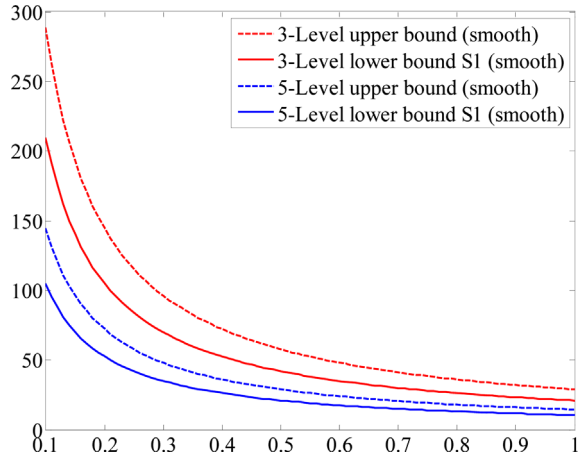

Fig. 12. (Color online) Smooth upper and lower bounds for three and five levels.

and 5 Levels.

Although the present paper is a review, several numerical simulations with the main topologies (CHB, NPC, FC) were carried out in this section in order to verify the Ruderman formulas. Simulations parameters are:

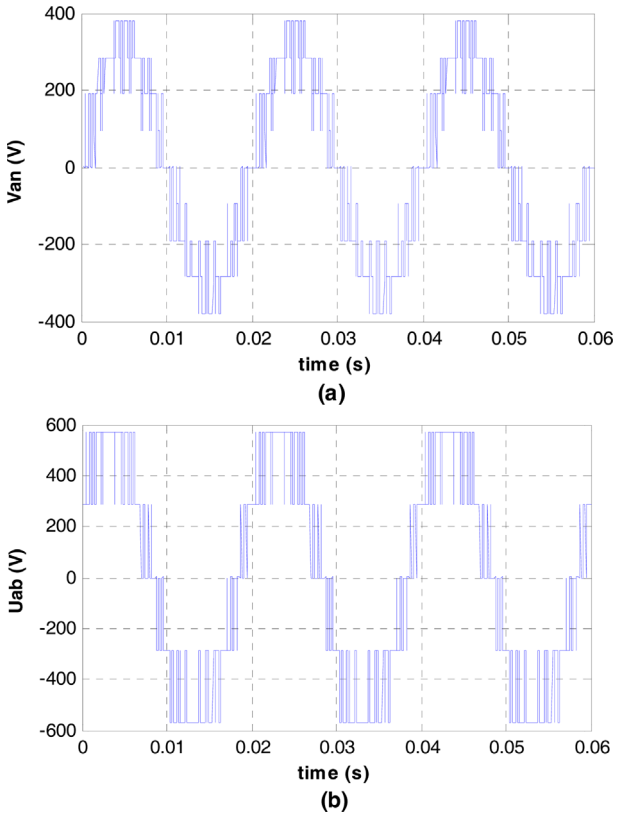

Fig. 13. (Color online) Five level CHB converter output voltage waveforms: (a) Phase voltage V_{an} and (b) line voltage U_{ab}.

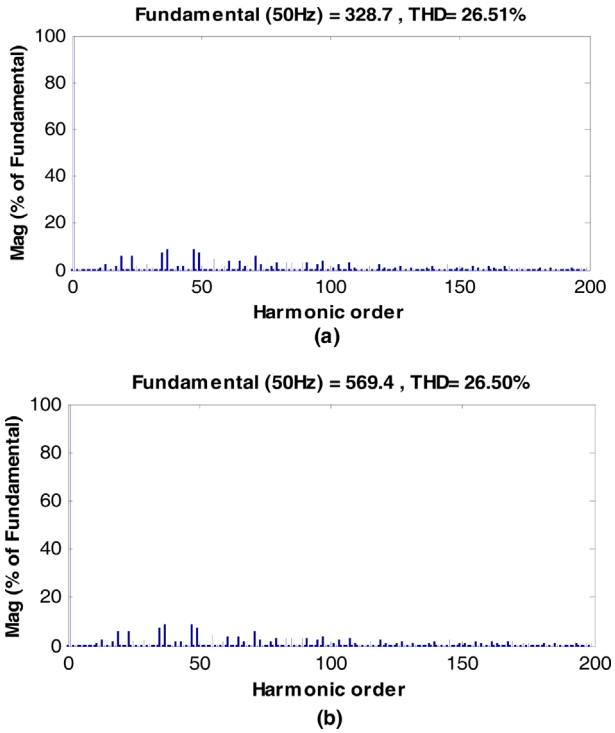

Fig. 14. (Color online) (a) Phase and (b) line harmonic spectrums of five level H-bridge.

- Frequency ratio: m_c = 100
- Sinusoidal wave: f_p = 50 Hz
- Carrier: f_m = 5 KHz.

After performing the necessary simulations, it was shown that the typical waves of the FC, NPC and H-bridge multilevel inverters (isolated neutral) are almost the same. To avoid repetition and space consuming, only output voltage waveforms as well as their harmonic spectrums relative to the CHB topology are reported in Fig. 13 and 14 in case of 5 levels. Instead, all simulation results are

Table 2. THD of line and phase voltages for five level CHB, NPC and FC inverters, M = 1.

	V_{an} THD%	U_{ab} THD%
CHB	26.51%	26.50%
NPC	26.91%	26.92%
FC	26.95%	26.96%

Table 3. Voltage quality bounds for five, seven and nine level H-Bridge inverters, M = 1.

	5 Levels	7 Levels	9 Levels
THD_{up}	28.85%	19.23	14.42%
THD_{low}	23.5%	15.66	11.75%
THD_{calc}	26.5%	18.38	13.55%

resumed in Tables 2 and 3.

Even if it is obvious that, the load phase voltage V_{an} has a number of levels significantly higher than U_{ab}, Fig. 13, the calculated THDs of line and phase voltages are quite similar whatever the multilevel converter is, Table 2.

Referring to (14) and (15), the upper and lower bounds are calculated for 5L and 9L H-bridge converters where an m cascaded multilevel converter operating under a modulation index M equal to 1 gives a line to line voltage with $L = (m\text{-}1)/2$ non negative levels [41]. Indeed, the estimated THD values are within the interval [THD_{up}, THD_{low}] as illustrated by Table 3, proving the veracity of the Ruderman formulas at least for M = 1.

6. Conclusion

This paper has reviewed the state of the art of multilevel inverters. Various multilevel topologies have been reviewed including major structures as well as their derived and hybrid ones. Despite the wide range of new multilevel configurations, they remain on the shadow of the basic topologies that are NPC, H-Bridge and FC. This work also investigated abundant modulation paradigms. The most relevant techniques for harmonic elimination, in order to improve the output voltage quality, are cited. The presented THD voltage formulas, given in the literature, are also reported and verified by appropriate simulations for some modulation indexes. It has to be emphasized that the choice of the convenient inverter type is a tradeoff which obviously depends on the application and the desired achievements.

References

[1] R. Portillo, R. Vasquez, J. I. Leon, and M. M. Prants, IEEE Trans. Industrial Informatics **9**, 1148 (2012).
[2] A. Lesnicar and R. Marquardt, IEEE Bologna Tech. Conference, Bologna, Italy (2003).
[3] R. H. Baker and L. H. Bannister, Electric Power Converter, U.S. Patent (3 867 643), (1975).
[4] A. Nabae, I. Takahashi, and H. Akagi, IEEE Trans. Ind. Appl. **17**, 518 (1981).
[5] T. Meynard and H. Foch, EPE J. **3**, 99 (1993).
[6] M. D. Manjrekar, P. Steimer, and T. A. Lipo, Conf. Rec. IEEE/IAS Annual Meeting, 1520 (1999).
[7] D. Zhong, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, Proceeding of Applied Power Electronics Conference and Exposition (APEC'06), 426 (2006).
[8] L. A. Serpa, Ph.D. Thesis, Swiss Federal Institute of Technology, Switzerland (2007).
[9] E. N. Abilguard and M. Moinas, Energy Procedia **20**, 227 (2012).
[10] E. Babaei, M. F. Kangarlu, M. Sabahi, and M. R. A. Pahlavani, Electric Power System Research **96**, 101 (2013).
[11] T. Brückner, T. Bernet, and H. Güldner, IEEE Trans. Ind. Electron. **52**, 855 (2005).
[12] T. Brückner, The active NPC converter for medium-voltage drive, Shaker Verlag (2005).
[13] D. Floricau, E. Floricau, and M. Dumitrescu, International School on Non sinusoidal Currents and Compensation, Lagow, Poland (2008).
[14] A. Leredde, G. Gateau, and D. Floricau, Proc. 35th Annual Conf. of IEEE Industrial Electronics IECON '09, 676 (2009.
[15] Y. Ounejjar, K. Al-Haddad, and L. A. Grégoire, IEEE Trans. Ind. Electron. **58**, 1294 (2011).
[16] E. Esfandiari and F. Mesrinejad, Journal of Circuits, Systems, and Computers **22**, 1 (2013).
[17] S. S. Fazel, Ph. D Thesis, Technische Universität, Berlin (2007).
[18] A. Lega, Ph.D. Thesis, University of Bologna, (2007).
[19] M. R. Islam, Y. G. Guo, and J. G. Zhu, IEEE Trans. Power. Electron. **29**, 4167 (2014).
[20] P. Veena, V. Indragandhi, R. Jeybharath, and V. Subramaniyaswamy, Renewable and Sustainable Energy Reviews **34**, 628 (2014).
[21] K. A. Tehrani, I. Rasoanarivo, and F. M. Sargos, Electric Power Systems Research **81**, 297 (2010).
[22] A. K. Gupta, Ph.D. Thesis, National University of Singapore, (2008).
[23] L. He, K. Zhang, J. Xiong, S. Fan, X. Chen, and Y. Xue, IEEE Applied Power Electronics Conference and Exposition, 799 (2015).
[24] X. Zha, L. Xiong, J. Gong, and F. Liu, Power Electronics IET **7**, 1313 (2014).
[25] N. P. Schibli, T. Nguyen, and A. C. A. Rufer, IEEE Trans. Power. Electron. **13**, 978 (1998).
[26] C. A. Martins, X. Roboam, T. A. Meynard, and A. S. Carvalho, IEEE Trans. Power. Electron. **17**, 286 (2002).
[27] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M.A. Perez, and J. I. Leon, IEEE Trans. Ind. Electron. **8**, 2553 (2010).
[28] J. Rodriguez, J. Pontt, G. Alzarnora, N. Becker, O. Einenekel, and A. Weinstein, IEEE Trans. Ind. Electron. **49**, 1093 (2002).
[29] M. Carpita, M. Marchesoni, M. Pellerin, and D. Moser, IEEE Trans. Ind. Electron. **55**, 2203 (2008).
[30] S. Dieckerhoff, S. Bernet, and D. Krug, IEEE Trans. Power. Electron. **20**, 1328 (2005).
[31] S. Rahmani and K. A. Al-Haddad, IEEE International Symposium on Industrial Electronics, 925 (2006).
[32] J. Wang and Y. Li, International Conference on Electrical Machines and Systems, 18 (2007).
[33] B. Gultekin and M. Ermis, IEEE Trans. Power. Electron. **28**, 4930 (2013).
[34] W. Song and A. Q. Huang, IEEE Trans. Ind. Electron. **57**, 2700 (2009).
[35] R. C. Portillo, M. M. Prants, J. I. Leon, J. A. Sanchez, J.

M. Carrasco, E. Galvan, and L. G. Franquelo, IEEE Trans. Ind. Electron. **53**, 1483 (2006).
[36] M. Malinowski, W. Kolomyjski, M. P. Kazmierkowski, and S. Stynski, IEEE International Conference on Industrial Technology, 1516 (2006).
[37] P. Karuppusamy and A. M. Natarajan, Journal of Circuits, Systems, and Computers, **24**, 1 (2015).
[38] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, and J. Balcells, IEEE Trans. Ind. Electron. **53**, 1504 (2006).
[39] S. Daher, J. Schmid, and F. L. M. Antunes, IEEE Trans. Ind. Electron. **55**, 2703 (2008).
[40] I. Colak,. E. Kabalci, and R. Bayindir, Energy Conversion and Management Elsevier **52** 1114 (2011).
[41] A. Ruderman, IEEE Trans. Ind. Electron. **62**, 1548 (2015).
[42] A. Ruderman, B. Reznikov, and S. Busquets-Monge, IEEE Trans. Ind. Electron. **60**, 1999 (2013).
[43] G. Mehlmann, A. Ruderman, and G. Herold, Proc. Int. Energy Conf. & Exhib., 90 (2012).
[44] A. Ruderman, G. Mehlmann, and B. Reznikov, Proc. Int. Conf. on Optim. of Electr. and Electron. Equip., 58 (2012).
[45] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, IEEE Trans. Ind. Electron. **57**, 2197 (2010).
[46] J. Rodriguez, J. S. Lai, F. Z. Peng, and M. A. Pérez, IEEE Trans. Ind. Electron. **49**, 724 (2002).
[47] D. Ostojic, Ph.D. Thesis, Facoltà Di Ingeneria (2010).
[48] S. Khomfoi and L. M. Tolbert, Chapter 17 Multilevel Power Converters, Third Edition of Power Electronics Handbook, Butterworth-Heinemann-Elsevier (2011).
[49] T. Wanjekeche, D. V. Nicolae, and A. A. Jimoh, J. Energy and Power Eng. **6**, 1335 (2012).
[50] M. D. Manjrekar and T. A. Lipo, Proc. of Applied Power Electronics Conference and Exposition **2**, 523 (1998).
[51] B. S. Suh, Y. H. Lee, D. S. Hyun, and T. A. Lipo, Proc. of European Conference on Power Electronics and Application, Lausanne, Switzerland (1999).
[52] D. A. Ruiz-Caballero, R. M. Ramos-Astudillo, S. A. Mussa, and M. L. Heldwein, IEEE Trans. Ind. Electron. **57**, 2307 (2010).
[53] M. Gutierrez, G. Venkataramanan, and A. Sundaram, Proc. of the IEEE Ind. Appl. Soc. Annual Meeting **1**, 359 (1999).
[54] A. S. Bahman, M. S. Thesis, Chalmers University of Technology, Sweden (2011).
[55] H. S. Patel and R. G. Hoft, IEEE Trans. Ind. Appl. **10**, 666 (1974).
[56] L. Song and Y. Manyuan, International Conference on Electronic & Mechanical Engineering and Information Technology **5**, 2738 (2011).
[57] F. Filho, L. M. Tolbert, Y. Cao, and B. Ozpineci, IEEE Energy Conversion Congress and Exposition, 594 (2010).
[58] M. Tamasas, M. Saleh, M. Sahker, and A. Hammoda, 7th IEEE Mediterranean Electrotechnical Conference, 17 (2014).
[59] H. Yang, H. Luo, P. Sun, C .Li, W. Li, and X. He, 29th Annual IEEE Applied Power Electronics Conference and Exposition, 2238 (2014).
[60] A. Gopinath, A. S. A. Mohamed, and M. R. Baiju, IEEE Trans Ind. Electron. **56**, 1230 (2009).
[61] A. K. Gupta and A. M. Khambadkone, IEEE Trans. Power. Electron. **22**, 517 (2007).
[62] J. H. Seo, C. H. Choi, and D. S. Hyun, IEEE Trans Power. Electron. **16**, 545 (2001).
[63] N. Celanovic and D. Boroyevich, IEEE Trans Ind. Appl. **37**, 637 (2001).
[64] A. R. Beig, G. Narayanan, and V. T. Ranganathan, IEEE Trans. Ind. Electron. **54**, 486 (2007).
[65] M. A. M. Prats, J. I. L. G. Van, R. P. Guisado, J. M. C. Solis, and L. G. Franquelo, Journal of Circuits, Systems, and Computers **13**, 845 (2004).