Multilevel Magnetization Switching in a Dual Spin Valve Structure

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Here, we describe a dual spin valve structure with distinct switching fields for two pinned layers. A device with this structure has a staircase of three distinct magnetoresistive states. The multiple resistance states are achieved by controlling the exchange coupling between two ferromagnetic pinned layers and two adjacent anti-ferromagnetic pinning layers. The maximum magnetoresistance ratio is 7.9% for the current-perpendicular-to-plane and 7.2% for the current-in-plane geometries, with intermediate magnetoresistance ratios of 3.9% and 3.3%, respectively. The requirements for using this exchange-biased stack as a three-state memory device are also discussed.

Keywords : GMR spin valve, multi-bit memory, dual spin valve, current-perpendicular-to-plane GMR

1. Introduction

The multilayered magnetic structure shows promise in high-density read heads, programmable logic devices, and nonvolatile magnetic random access memory (MRAM) applications [1-3]. The basic element of the magnetic multilayer structure is the spin valve (SV), which consists of the following sequence of layers: antiferromagnetic layer/pinned ferromagnetic layer/nonmagnetic Cu-spacer layer/free ferromagnetic layer. For complete independent magnetization switching of the pinned and free layers at different applied magnetic fields, the ferromagnetic pinned layer is exchange coupled to the antiferromagnetic layer in order to effectively pin the orientation of the magnetization. By applying a small magnetic field, the magnetization direction of the free ferromagnetic layer will change to align with the direction of the field. Two resistance (R) states can be obtained depending on the relative orientation of the magnetizations of the two ferromagnetic layers. The giant magnetoresistance (GMR) ratio is defined as $(R_{ap}-R_p)/R_p$, where R_p and R_{ap} are the resistances when the magnetizations of the two ferromagnetic layers are aligned in parallel or anti-parallel. Accordingly, a binary code (one bit) of information is stored in an SV cell by analyzing the magnetization configuration

of each layer (i.e., "0" for R_p and "1" for R_{ap}).

MRAM has many advantages over the conventional memory devices, including nonvolatility, random access, memory data retention, and fast reading and writing performance. One of the major disadvantages of MRAM, however, is the relatively low storage density. In order to compete with other memory devices, therefore, the storage density of the MRAM must be increased. This is usually achieved by reducing the cell size. The smaller cell, however, requires a larger switching field because a large demagnetizing field arises from the poles of the nanometer-sized cell edge, leading to large write currents. Another method is to increase the number of memory states by increasing the number of resistance states in a cell. Binary memory states are currently predominant but multistate memory has been receiving great attention because it offers excellent storage density [4-6]. The possibility of fabricating a multilevel signal storing magnetic device has been recently demonstrated. However, it is difficult to use in practice because of the lower operating temperature, lower coercivity, and electrical connection of cells.

In this study, we adopt a different approach by using a dual spin valve (DSV) structure with current-perpendicular-to-plane (CPP) geometry to create a multibit memory cell. The main advantage of the CPP-DSV structure is that the free layer has complete, independent magnetization switching – the two pinned layers can be made to switch at different applied magnetic fields (multiple resistance states)

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by controlling the exchange coupling between the two pinned ferromagnetic layers and the two antiferromagnetic pinning layers with an increased GMR ratio and a decreased cell size (i.e. an increase in density). The multiple-storage level feature is expected to drastically improve the storage capability of MRAM.

2. Experimental Methods

Multilayered magnetic structures were prepared using a Sputtered Films Inc. "Shamrock" deposition tool with a typical base pressure of less than 3×10^9 mbar. The free and pinned layer easy axes were aligned along the same direction by applying a 10 mT magnetic field during deposition. Post-deposition annealing was carried out *ex situ* at 250 °C in a 5×10^8 mbar vacuum under an applied field of 800 mT for 2 h. An electromagnetic probe station capable of generating a magnetic field of ± 180 mT was used to measure the magnetoresistive properties of the DSVs. Current-in-plane (CIP) measurements were carried out using a standard four-point probe technique in a linear geometry. A current of 1 mA, applied parallel to the field, was used to probe the resistance as a function of the applied magnetic field. CPP measurements were carried out on nanopillar samples fabricated by electron beam lithography in a FEI Dual Beam system operating at 30 kV. Devices of 250 nm × 400 nm were fabricated using a TOK negative e-beam resist at a dose of 30 µC/cm². Post-exposure lift-off was carried out after Al_2O_3 deposition to insulate the top and bottom contacts. A top contact of Ta 5/Ag 50/Ta 5 (nm) was deposited by sputtering and subsequent lift off. The magnetic properties of the DSV structure were characterized using a Quantum Design Inc. superconducting quantum interference device (SQUID) magnetometer.

3. Results and Discussion

Before implementing the DSV structure, we characterized the antiferromagnetic/ferromagnetic thickness dependence of the exchange coupling of SiO_2/buffer [Ta 5/NiFe 3.5]/CoFe 5/Cu 2.8/CoFe t_1/IrMn t_2/Ta 5 (nm) and SiO_2/buffer [Ta 5/CoFe 3/Cu 3]/IrMn t_3/CoFe t_4/Cu 2.8/CoFe 5/Ta 5 (nm) for top and bottom pinned single SV structures, respectively. For top and bottom pinned single SV structures, we used different buffer layers. One of the main reasons for using a different buffer layer is to control the SV texture, as the development of SV texture depends on the buffer layer and different exchange coupling strengths are shown depending on the SV texture. Normally, the exchange coupling strength is inversely proportional to

the ferromagnetic layer thickness. We found that decreasing the thickness of the pinned CoFe layer to below 1.5 nm reduces the GMR ratio. Therefore, a value of around 1.5 nm is the optimal thickness for the pinned ferromagnetic layer, providing both a high exchange coupling and GMR ratio.

We have also measured the dependence of the exchange coupling on the antiferromagnetic thickness. Exchange biasing occurred when the antiferromagnetic layer thickness was 4 nm and continued to increase as the layer thickness increased up to 10 nm. When the antiferromagnetic IrMn thickness was below 4 nm, no exchange bias occurred. Previous experiments have shown that the exchange bias decreases with decreasing antiferromagnetic thickness and that a critical thickness of the antiferromagnetic layer is needed to develop exchange coupling. If the antiferromagnet is very thin, the anisotropy energy of the IrMn layer is lower than the exchange coupling energy; therefore, when the pinned ferromagnetic magnetization layer rotates due to the applied magnetic field, the antiferromagnetic IrMn magnetization follows the ferromagnetic layer resulting in zero exchange coupling [7]. The rapid increase in exchange coupling as the IrMn thickness is increased above 4 nm is due to the increase in the magnetic order of the IrMn layer, which results in the enhancement of domain wall stability with increasing thickness [8]. The exchange coupling decreases again when the IrMn thickness increases above 10 nm. The decrease in the exchange coupling with an increase in the antiferromagnetic thickness is caused by domain walls that are more difficult to form since they are oriented perpendicular to the interface extending through the whole antiferromagnetic layer [9, 10].

According to the dependence of the exchange bias and the magnetoresistance (MR) measurements on the antiferromagnetic and ferromagnetic layer thicknesses, the optimized thickness of the CoFe layer is 2.0 nm, and those of the IrMn bottom and top pinned layers are 6 nm and 10 nm, respectively. Fig. 1 shows the data for an optimized structure with SiO_2/buffer [Ta 5/NiFe 3.5]/CoFe 5/Cu 2.8/CoFe 2/IrMn 10/Ta 5 (nm) and SiO_2/buffer [Ta 5/CoFe 3/Cu 3]/IrMn 6/CoFe 2/Cu 2.8/CoFe 5/Ta 5 (nm) for both top and bottom pinned single SV structures, respectively. As shown in this figure, the exchange biasing value was much higher in the bottom pinned structure then in the top pinned structure. One of the main reasons for this larger exchange coupling, in our system, is associated with an increase in the (111) FCC texture because of using the CoFe and Cu buffer layer [11].

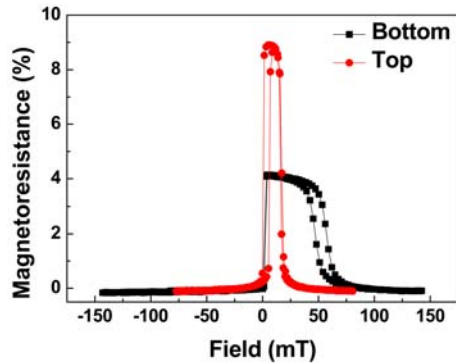Fig. 2 shows scanning electron microscopy (SEM) images of typical structures that we used in this study (top view)

Fig. 1. (Color online) Data for an optimized structure with SiO$_2$/Ta 5/NiFe 3.5/CoFe 5/Cu 2.8/CoFe 2/IrMn 10/Ta 5 (nm) and SiO$_2$/Ta 5/CoFe 3/Cu 3/IrMn 6/CoFe 2/Cu 2.8/CoFe 5/Ta 5 (nm) as the top and bottom pinned layers of the single spin valve structure, respectively.
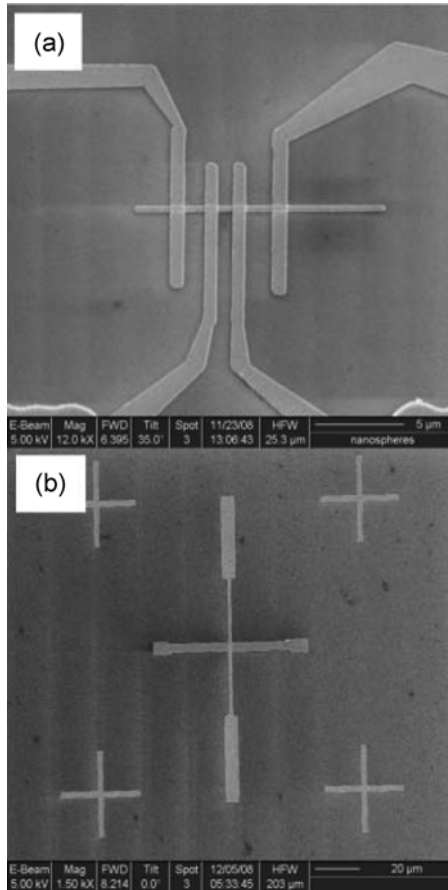

Fig. 2. A scanning electron microscopy (SEM) image of a typical structure used in this study (top view) for (a) CIP SV and (b) CPP SV geometry.

for (a) CIP SV and (b) CPP SV geometry. Devices of 360 nm × 10 μm are fabricated for CIP SV, and the inter-probe distance was less than 1.2 μm. Devices of 250 nm × 400 nm nanopillars are fabricated for CPP SV.
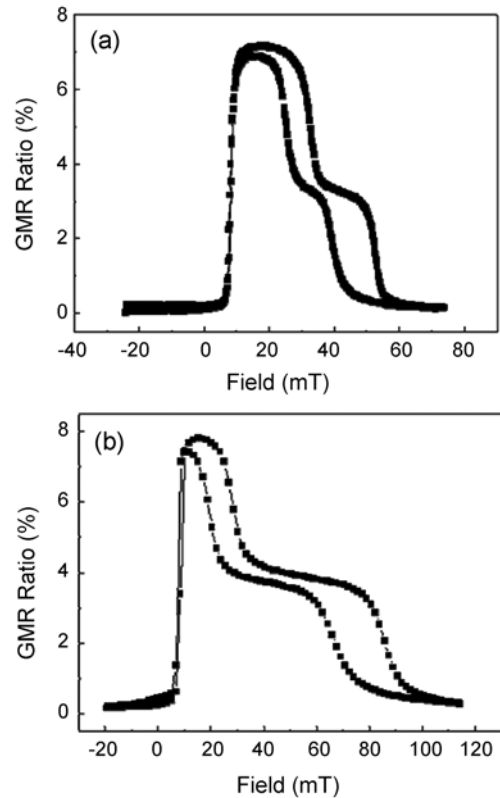

Fig. 3. The MR curve with (a) CIP and (b) CPP geometry. The sample was patterned onto (a) a 360 nm × 10 μm nanowire and (b) a 250 nm × 400 nm nanopillar as described in the text. Both curves show the stability of the intermediate state in the presence of an applied field.

To satisfy the distinctly different requirements of the exchange coupling strength and GMR ratio, we incorporated the results for the single SV into the DSV structures. The DSV composition was as follows: Si/SiO$_2$/Ta 5/CoFe 3/Cu 3/IrMn 6/CoFe 2/Cu 2.8/CoFe 2.5/Cu 2.8/CoFe 2/ IrMn 10/ Ta 5 (nm). The results for the DSV structure are shown in Fig. 3; the thicknesses of the two ferromagnetic CoFe pinned layers and the antiferromagnetic IrMn pinning layers were varied so as to yield distinctly different exchange bias fields. The DSV structure clearly exhibits three states with different resistance values.

Fig. 3(a) shows the MR-H curve and the magnetization switching behaviors in the CIP geometry, from which the magnetization switching of each layer can be clearly distinguished. Starting from the negative saturation field, the magnetization directions of all layers were parallel to the applied field, which results in minimum resistance. As the positive field was increased to nearly 5 mT, the resistance dramatically increased because the magnetization direction of the central free layer reversed to an antiparallel orientation with respect to that of both pinned

layers, resulting in maximum resistance. As the negative field is increased to approximately 30 mT, the magnetization direction of the top pinned CoFe layer started to reverse and aligned parallel with the free layer but antiparallel to the bottom pinned CoFe layer, resulting in intermediate resistance. Since the bottom pinned CoFe layer had a higher exchange bias than the top pinned CoFe layer, which was characterized in Fig. 1, it was possible to tune the exchange coupling strength to yield well-separated switching fields for both pinned layers. This allowed the intermediate resistance state to exist. By increasing the applied magnetic field beyond 50 mT, the magnetization direction of the bottom pinned CoFe layer rotated toward an orientation parallel to that of the free and top pinned CoFe layers, again resulting in a low resistance state.

The results obtained for the DSV in the CPP geometry in a 250 nm × 400 nm nanopillar are shown in Fig. 3(b). In the CPP configuration, the GMR ratio was increased from 7.2% (for the CIP configuration) to 7.9%. The higher GMR ratio in the CPP configuration is related to the fact that the spin diffusion length is the important parameter in this geometry, and the electrons are forced to cross all interfaces during transport through the device. In the CIP case, the important parameter is the mean free path of conduction electrons because the current is shunted by the normal metal layer, which cannot contribute to GMR.

For clarity, the three MR states, which yield three memory states, can be considered as corresponding to "0," "1," and "2" in terms of memory storage. Multiple resistance states allow drastic improvement in the storage capability per unit cell compared to that of a conventional single bit memory cell, which has only two resistance states. Although multiple resistance states were achieved in our device by optimizing the exchange coupling between the two ferromagnetic pinned layers and the two antiferromagnetic pinning layers, the structure in its present form cannot operate as a multibit memory because only two of the three states are stable at zero magnetic field. The intermediate resistance state is only accessible in an applied field. Even if the two pinned layers were pinned in opposite directions, there would be only two storage states, corresponding to the two orientations of the free layer. In order to achieve multilevel storage in this type of structure, at least one of the antiferromagnetic pinning layers has to be removed. It has been demonstrated previously, using three free layers with differing coercivities, that a multilevel memory device can be constructed without exchange pinning. If just one of the pinning layers is removed, we have a DSV with two free layers, one half of the device forming an exchange-biased SV and the other half forming a pseudo-SV with two switchable layers having different coercivities.

4. Conclusion

A DSV was built with exchange bias on the top and bottom pinned layers and a free central layer. By selecting antiferromagnetic and ferromagnetic layers of appropriate thickness, it was possible to separate the three magnetization switching fields and produce a staircase magnetoresistive curve. Multiple resistance states were achieved by controlling the exchange coupling between the two ferromagnetic pinned layers and the two adjacent antiferromagnetic pinning layers. The maximum magnetoresistance ratio was 7.9% for CPP and 7.2% for CIP geometries with intermediate magnetoresistance values of 3.9% and 3.3%, respectively. In its present form, the structure has no application as a multibit memory device since the intermediate resistance state is only stable in an applied field. However, if either the top or bottom pinned layer is unpinned, it could switch about zero like the free layer, and a four-state DSV structure could be achieved.

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